OSD32MP15x Datasheet

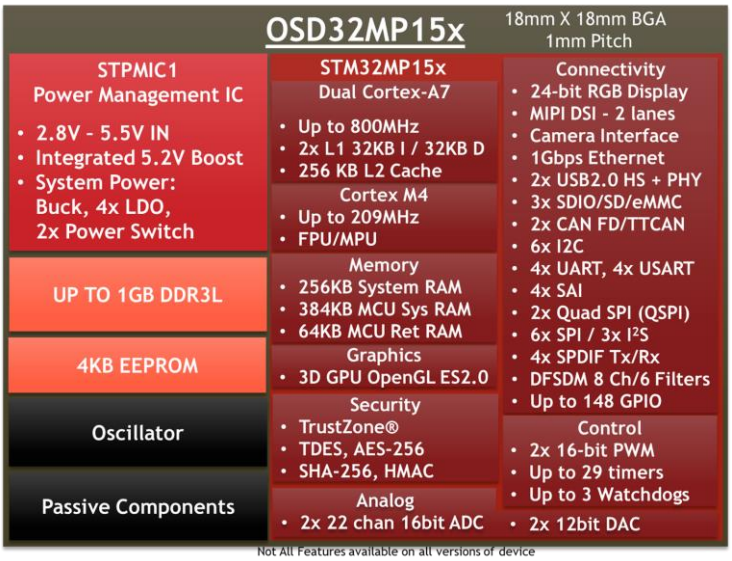
Rev. 11 3/31/2026

Introduction

The OSD32MP15x System-in-Package (SiP) devices deliver all the power of a Microprocessor in a package that feels like a Microcontroller in the smallest possible footprint.

At their core, the OSD32MP15x devices have the versatile STMicroelectronics STM32MP15x featuring Dual Arm® Cortex® A7 Cores and an Arm® Cortex® M4. Along with the processor, the OSD32MP15x integrates up to 1GB of DDR3L, STPMIC1 Power Management IC, EEPROM, MEMs Oscillator, and passives into a single easy to use BGA package.

This integration enables fastest designs with the STM32MP15x by removing the tedious tasks that do not add value to an end system while allowing low cost-manufacturing and miniaturized products.



OSD32MP15x Block Diagram

Features

- ST STM32MP15x, DDR3L, STPMIC1A, 4KB EEPROM, Oscillator and passive components integrated into a single package
- STM32MP15x Features:
  - Arm® Cortex®-A7 up to 800MHz x2
  - Arm® Cortex®-M4 up to 209MHz
  - NEON™SIMD Coprocessor x2
  - Arm® TrustZone®
  - USB 2.0 HS + PHY x2
  - Ethernet 10/100/1000
  - CAN FD/TTCAN x2, UART x4, USART x4, SPI x6, I2C x6, I2S x3, QSPI x2
  - eMMC/SD/SDIO Ports x3
  - GPIO x148
  - 24-bit RGB Display, MIPI DSI
  - Camera Interface
  - 22 Channel 16-bit ADC x2, 12-bit DAC x2
  - Configurable I/O voltage (1.8V - 3.3V)
- Access to all Signals of the STM32MP1 TFBGA 361 Package
- Up to 1GB DDR3L
- Low Power MEMS Oscillator
- Single Voltage Input: 2.8V-5.5V
- Integrated Boost: 5.2V
- System Power: Buck, Boost, LDOx4, Power Switch x2

Benefits

- Integrates over 100 components
- Compatible with STM32MP1 development tools and software
- Significantly reduces design time
- Up to 64% reduction in board space vs discrete implementation
- Decreases layout complexity
- Wide BGA ball pitch allows low-cost assembly
- Simplifies component sourcing
- Increased reliability through reduced number of components

Package

- 18mm X 18mm BGA
- 302 Ball, 1mm Pitch
- Temp Range: 0 to 85°C, -40 to 85°C

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1 Revision History

Revision Number	Revision Date	Changes	Author
1.0	2/25/2020	Initial Revision for Production Device	Greg Sheridan, Erik Welsh, Neeraj Dantu, Eshtaartha Basu
1.1	4/6/2020	Update Electrical Characteristics, minor additions to references and pin descriptions	Neeraj Dantu
2.0	8/28/2020	Rotated Ball Map so that A1 is now in the top left corner. Added references to the default DDR configuration register settings and the $VIN_{OK_Threshold}$ Updated comment for PMIC_PONKEYN signal. Updated Figure 7.1	Greg Sheridan
3.0	9/17/2020	Added Different Processor Variations, Clarified VDD connection requirements	Greg Sheridan
4.0	1/29/2021	Added information on 1.8V operation, Landing Pad Size, and Differences between the STM32MP1 processors. Updated Reference Documents.	Greg Sheridan
5.0	6/15/2021	Added Extended Temperature Option, and reference to the Thermal Guide	Greg Sheridan
6.0	02/02/2022	Updated sections 7.6.7, 7.6.8, and 7.6.9	Eshtaartha Basu
7.0	11/30/2022	Added PMIC I2C address, Added a Note in the Processor Comparison section	Eshtaartha Basu, Greg Sheridan
8.0	08/09/2024	Updated Figure 7.2 to remove the connection of NRST_CORE	Neeraj Dantu
9.0	12/1/2024	Updated Storage Requirements and footnote for Table 2-3	Greg Sheridan
10	1/20/2026	Updated DDR section to point to github for DDR parameters	Neeraj Dantu, Greg Sheridan
11	3/31/2026	Added Note to Operating Conditions table about requirements to support full 2000mA load.	Matt Schuldt

NOTICE: These devices are susceptible to moisture and are classified as **MSL 4**. Ensure you are following the guidelines in the **Storage Requirements** section in this document.

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2 Block Diagram

The OSD32MP15x devices consist of six (6) main components serving five (5) distinct functions. The main processor is the STM32MP15x from STMicroelectronics featuring dual core Arm® Cortex®-A7 running up to 800MHz and an Arm® Cortex® M4 at 209MHz. The power system consists of the STPMIC1A Power Management IC (PMIC). The system memory includes up to 1GB DDR3L. A 4KB EEPROM provides nonvolatile memory for configuration. Finally, there is a low power, low jitter, highly stable MEMS CMOS Oscillator. It is used for the primary clock input (HSE). Figure 2.1 shows a detailed block diagram of the OSD32MP15x and breaks out the key functions of the STM32MP15x processor.

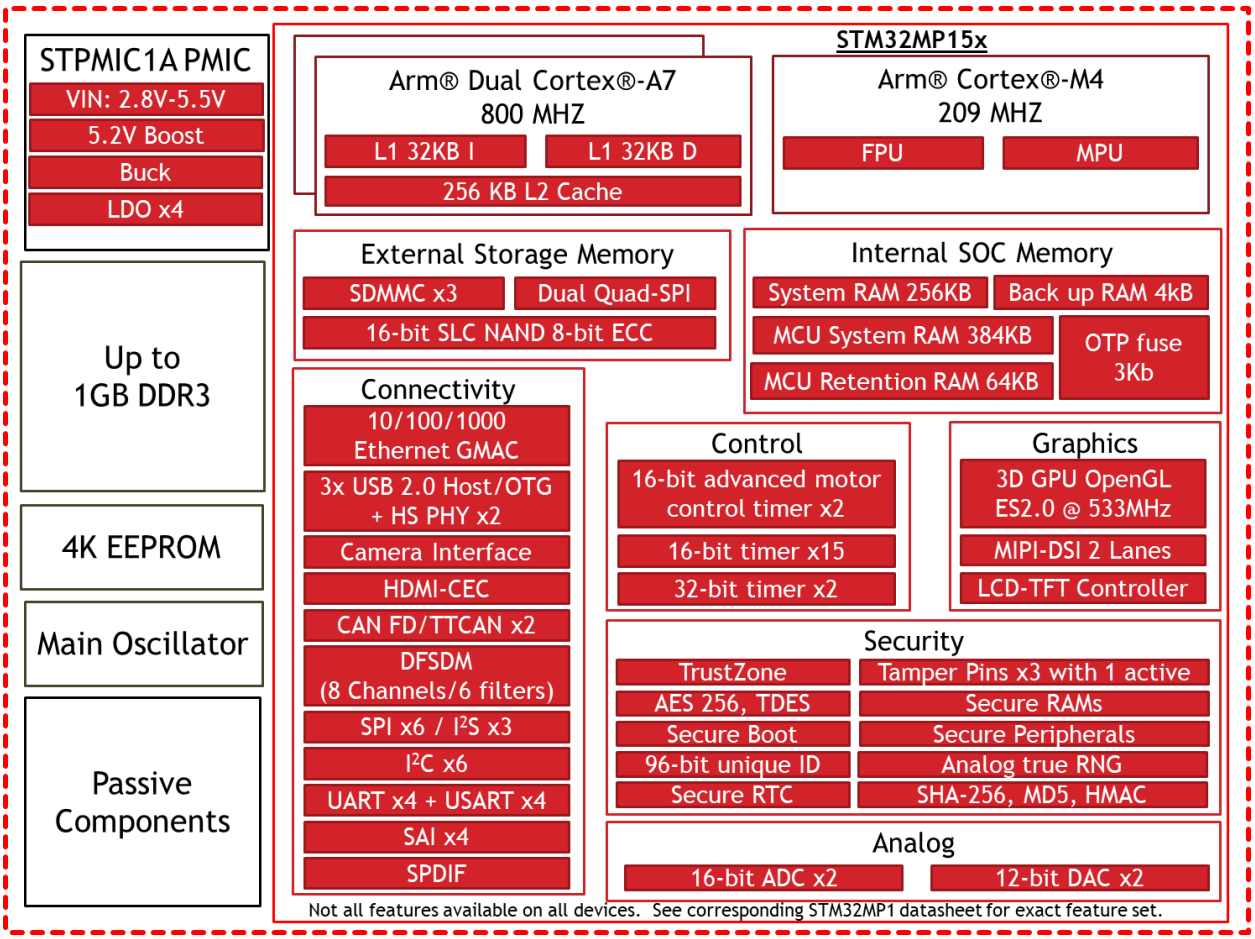

Figure 2.1 - OSD32MP15x Detailed Block Diagram

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2.1 Processor Comparison

The OSD32MP15x family supports all variations of the STM32MP1 microprocessor series with dual Arm® Cortex®-A7 and Cortex®-M4 Cores from STMicroelectronics. They are all pin compatible except for where the function does not exist on that particular variation. Refer to Table 2-1 for the differences between the different processor variations.

Table 2-1 - STM32MP1 Processor Comparison

STM32MP1 Devices	Cortex®-A7 Cores	CPU Max Frequency (MHz)	Cortex®-M4 Cores	MCU Max Frequency (MHz)	3D GPU	GPU Max Frequency	HW Crypto	FD-CAN	MIPI®-DSI
STM32MP157C	2	650	1	209	✓	533	✓	2	✓
STM32MP157F	2	800	1	209	✓	533	✓	2	✓
STM32MP157A	2	650	1	209	✓	533	-	2	✓
STM32MP157D	2	800	1	209	✓	533	-	2	✓
STM32MP153C	2	650	1	209	-	-	✓	2	-
STM32MP153F	2	800	1	209	-	-	✓	2	-
STM32MP153A	2	650	1	209	-	-	-	2	-
STM32MP153D	2	800	1	209	-	-	-	2	-

See Section 3 Product Number Information for available processor variants.

2.2 Passives

Besides the six major components, the OSD32MP15x also integrates capacitors, resistors, inductors, and ferrite beads (Passives). Table 2-2 and Table 2-4 lists the equivalent capacitance and resistance integrated into the OSD32MP15x. This includes the approximate bulk capacitance on input and output power rails as well as all pull-up resistor locations and values.

Table 2-3 outlines the recommended external bulk capacitance that should be included externally on the system power output rails only if they are being used. No other external decoupling / bypass capacitors are needed in most applications.

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Table 2-2 - OSD32MP15x Capacitors (Approximate Bulk Capacitance)

From	To	Device	Description	Type	Value
VIN	DGND	STPMIC1	VIN input capacitance	C	25uF
PMIC_BSTIN	DGND	STPMIC1	PMIC_BSTIN input capacitance	C	4.7uF
PMIC_LDO25IN	DGND	STPMIC1	VIN_BAT input capacitance	C	1uF
PMIC_VOUT4	DGND	STPMIC1	PMIC_VOUT4 output capacitance	C	22uF
PMIC_BSTOUT	DGND	STPMIC1	PMIC_BSTOUT output capacitance	C	10uF
PMIC_SWOUT	DGND	STPMIC1	PMIC_SWOUT output capacitance	C	4.7uF
PMIC_LDO1	DGND	STPMIC1	PMIC_LDO1 output capacitance	C	4.7uF
PMIC_LDO2	DGND	STPMIC1	PMIC_LDO2 output capacitance	C	4.7uF
PMIC_LDO5	DGND	STPMIC1	PMIC_LDO5 output capacitance	C	4.7uF
PMIC_LDO6	DGND	STPMIC1	PMIC_LDO6 output capacitance	C	4.7uF

Table 2-3 - OSD32MP15x Recommended Capacitors (Approximate Bulk Capacitance)*

From	To	Device	Description	Type	Value
PMIC_BSTIN	DGND	STPMIC1	PMIC_BSTIN input capacitance	C	4.7uF
PMIC_BSTOUT	DGND	STPMIC1	PMIC_BSTOUT output capacitance	C	10uF(1)
PMIC_VBUSOTG	DGND	STPMIC1	PMIC_VBUSOTG output capacitance	C	4.7uF(1)
PMIC_SWIN	DGND	STPMIC1	PMIC_SWIN input capacitance	C	4.7uF
PMIC_SWOUT	DGND	STPMIC1	PMIC_SWOUT output capacitance	C	4.7uF(1)

* Capacitors only needed if the given power rail is being used.

(1) If the power rail is being used to power a USB host port, a 100uF capacitance is recommended close to the connector. Additionally, a power switch with adjustable slew rate control to avoid in-rush over current is recommended

Table 2-4 - OSD32MP15x Resistors (Pull-ups / Pull-downs)

From	To	Device	Description	Type	Value
PDR_ON	VDD	STM32MP15x	PDR_ON input pull-up	R	10K Ohm
PDR_ON_CORE	VDD	STM32MP15x	PDR_ON_CORE input pull-up	R	10K Ohm
PZ4/PMIC_SCL	VDD	STM32MP15x	I2C4 SCL pull-up	R	1.5K Ohm
PZ5/PMIC_SDA	VDD	STM32MP15x	I2C4 SDA pull-up	R	1.5K Ohm
EEPROM_WP	VDD	EEPROM	EEPROM WP pull-up	R	10K Ohm

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3 Product Number Information

Figure 3.1 shows an example of an orderable product number for the OSD32MP15x family. This section explains the different sections of the product number. It also lists the valid entries and their meaning for each designator.

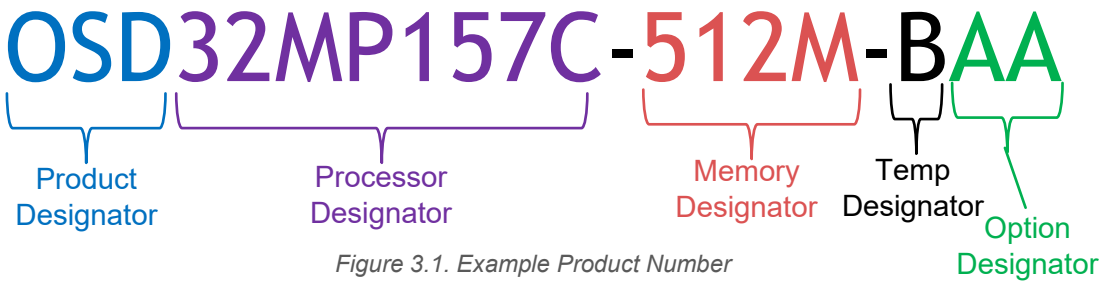

Figure 3.1. Example Product Number

Product Designator – Three letters that designate the family of device.

Table 3-1 - Family Designator

Family Designator	Product Line
OSD	OSD Product Line.

Processor Designator – A set of letters and numbers that designate the specific processor in the device. Table 3-2 shows the valid values for the Processor Designator.

Table 3-2 - Processor Designators

Processor Designator	Processor
32MP157C	ST Microelectronics STM32MP157C
32MP157F	ST Microelectronics STM32MP157F
32MP153C	ST Microelectronics STM32MP153C
32MP153A	ST Microelectronics STM32MP153A

Note: It is possible for the STM32MP1 in the OSD32MP1 to identify as a device that is a superset of the device marked on the package. For example, the STM32MP1 in an OSD32MP15**7C** could identify as the superset device STM32MP15**7F** but it would never identify as a STM32MP15**7A**. The performance, functionality, and temperature range of the device is guaranteed to the specification of the device marked on the package.

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Memory Designator – A set of letters and numbers that designate the DDR3L memory size in the device. Table 3-3 shows the valid values for the Memory Designator.

Table 3-3 - Memory Designator

Memory Designator	DDR Memory Size
1G	1GB x32 DDR3L
512M	512MB x16 DDR3L

Temp Designator – A letter or number that designates the operating case temperature range of the device. Table 3-4 shows the valid values for the Temp Designator.

Table 3-4 - Temp Designator

Temp Designator	Temperature Range
B	Commercial: 0 to 85°C
I	Industrial: -40 to 85°C (Not Available in F Variants)
E	Extended: -20 to 85°C (Available only in F Variants)

Option Designator – A set of two letters or numbers that designates the set of features in the device. Table 3-5 shows the valid values for the Option Designator unique for the OSD32MP15x devices.

Table 3-5 - Option Designator

Option Designator	Device Options
AA	24MHz Main Oscillator, 4KB EEPROM

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4 Reference Documents

4.1 Data Sheets

Below are links to the data sheets for the key devices used in the OSD32MP15x. Please refer to them for specifics on that device. The remainder of this document will describe how the devices are used in the OSD32MP15x system. It will also highlight any differences between the performance stated in the device specific datasheet and what should be expected from its operation in the OSD32MP15x.

- Processor

Processor Version	Datasheet
STM32MP157C	https://www.st.com/resource/en/datasheet/stm32mp157c.pdf
STM32MP157F	https://www.st.com/resource/en/datasheet/stm32mp157f.pdf
STM32MP153C	https://www.st.com/resource/en/datasheet/stm32mp153c.pdf
STM32MP153A	https://www.st.com/resource/en/datasheet/stm32mp153a.pdf

- PMIC STPMIC1 https://www.st.com/resource/en/datasheet/stpmic1.pdf
- EEPROM 24AA32A http://www.microchip.com/wwwproducts/en/24AA32A

4.2 Other References

This section contains links to other reference documents that could be helpful when using the OSD32MP15x device. Some are referenced in this document.

- STM32MP1 Reference Manual
  https://www.st.com/resource/en/reference_manual/dm00366349-stm32mp151-advanced-armbased-32bit-mpus-stmicroelectronics.pdf
- STM32MP1 SoC Errata
  https://www.st.com/resource/en/errata_sheet/dm00516256-stm32mp151x3x7x-device-errata-stmicroelectronics.pdf
- STM AN2639 – Handling & Process Recommendations
  https://www.st.com/resource/en/application_note/cd00173820.pdf
- OSD32MP15x Layout Guide
  https://octavosystems.com/app_notes/osd32mp15x-layout-guide/
- OSD32MP15x CubeMX Configuration Guide
  https://octavosystems.com/app_notes/stm32mp1-cubemx-tutorial-for-osd32mp15x/
- OSD32MP15x Thermal Guide
  https://octavosystems.com/app_notes/osd32mp15x-thermal-guide/
- DDR configuration on STM32MP1 Series MPU
  https://www.st.com/resource/en/application_note/dm00505673.pdf
- STPMIC1 Non-Volatile Memory Programming Guide
  https://octavosystems.com/app_notes/stpmic1-non-volatile-memory-programming-guide/
- STM32MP1 Hardware Design Getting Started
  https://www.st.com/resource/en/application_note/dm00389996.pdf

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5 Ball Map

The pins on the OSD32MP15x belong to four (4) distinct categories, STM32MP15x signals, STPMIC1A signals, control signals for internal components and Power Domains. The signal names for the STM32MP15x and the STPMIC1A have been named so they can be easily cross-referenced to the corresponding pin in the ST Datasheet.

All STM32MP1 signals on the OSD32MP15x Ball Map match the signal names of the STM32MP15x datasheet.

All the STPMIC1A signals have the prefix PMIC_ then the STPMIC1A signal name from the ST Datasheet.

Some of the control signals for the processor and PMIC and connected internally but can still be accessed outside of the OSD32MP15x. These signals have both the processor pin name and the PMIC pin name. For example: PZ5/PMIC_SDA.

The arrangement of the signals has been optimized for easy escape of the BGA. Table 5-1 through Table 5-5 show the ball map for the OSD32MP15x. Figure 5.1 illustrates how the different functions are grouped across the ball map.

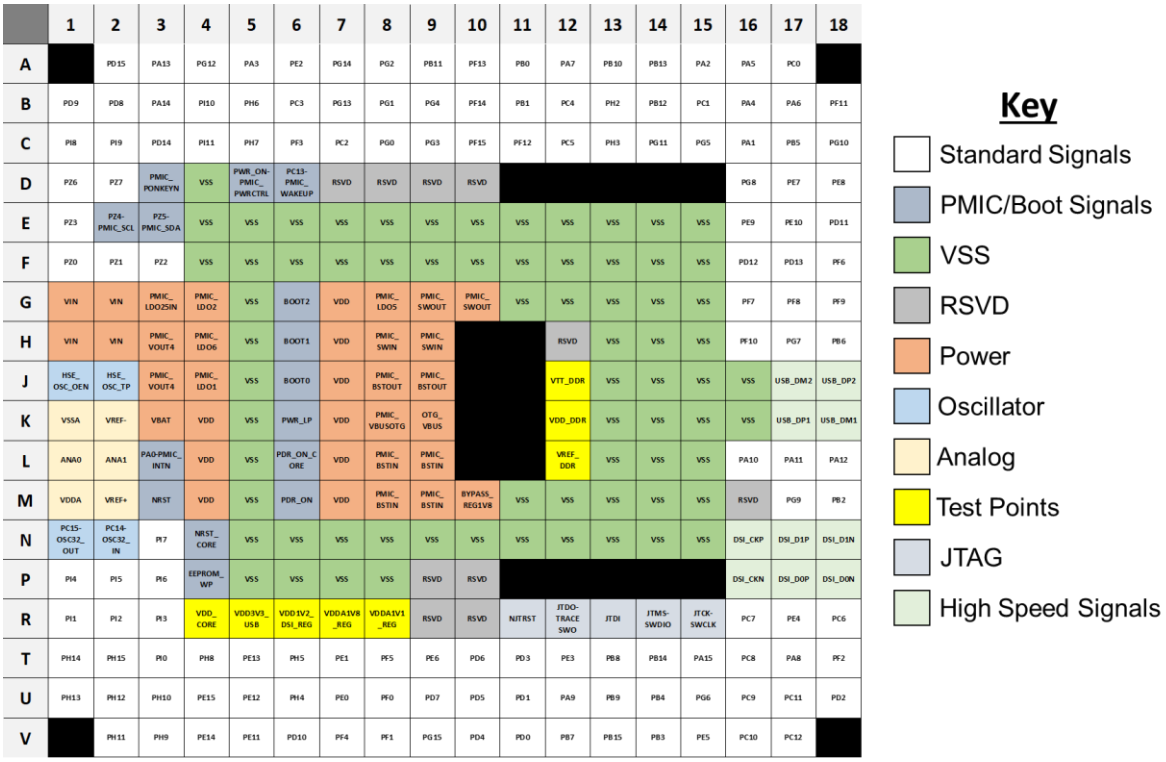

Figure 5.1. Ball Map Function Grouping

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Table 5-1 - OSD32MP15x Ball Map Top View (Columns A-D)

	1	2	3	4
A		PD15	PA13	PG12
B	PD9	PD8	PA14	PI10
C	PI8	PI9	PD14	PI11
D	PZ6	PZ7	PMIC_PONKEYN	VSS
E	PZ3	PZ4/PMIC_SCL	PZ5/PMIC_SDA	VSS
F	PZ0	PZ1	PZ2	VSS
G	VIN	VIN	PMIC_LDO25IN	PMIC_LDO2
H	VIN	VIN	PMIC_VOUT4	PMIC_LDO6
J	HSE_OSC_OEN	HSE_OSC_TP	PMIC_VOUT4	PMIC_LDO1
K	VSSA	VREF-	VBAT	VDD
L	ANA0	ANA1	PA0/PMIC_INTN	VDD
M	VDDA	VREF+	NRST	VDD
N	PC15-OSC32_OUT	PC14-OSC32_IN	PI7	NRST_CORE
P	PI4	PI5	PI6	EEPROM_WP
R	PI1	PI2	PI3	VDD_CORE
T	PH14	PH15	PI0	PH8
U	PH13	PH12	PH10	PE15
V		PH11	PH9	PE14

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Table 5-2 - OSD32MP15x Ball Map Top View (Columns E-H)

	5	6	7	8
A	PA3	PE2	PG14	PG2
B	PH6	PC3	PG13	PG1
C	PH7	PF3	PC2	PG0
D	PWR_ON/PMIC_PWRCTRL	PC13/PMIC_WAKEUP	RSVD	RSVD
E	VSS	VSS	VSS	VSS
F	VSS	VSS	VSS	VSS
G	VSS	BOOT2	VDD	PMIC_LDO5
H	VSS	BOOT1	VDD	PMIC_SWIN
J	VSS	BOOT0	VDD	PMIC_BSTOUT
K	VSS	PWR_LP	VDD	PMIC_VBUSOTG
L	VSS	PDR_ON_CORE	VDD	PMIC_BSTIN
M	VSS	PDR_ON	VDD	PMIC_BSTIN
N	VSS	VSS	VSS	VSS
P	VSS	VSS	VSS	VSS
R	VDD3V3_USB	VDD1V2_DSI_REG	VDDA1V8_REG	VDDA1V1_REG
T	PE13	PH5	PE1	PF5
U	PE12	PH4	PE0	PF0
V	PE11	PD10	PF4	PF1

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Table 5-3 - OSD32MP15x Ball Map Top View (Columns J-M)

	9	10	11	12
A	PB11	PF13	PB0	PA7
B	PG4	PF14	PB1	PC4
C	PG3	PF15	PF12	PC5
D	RSVD	RSVD		
E	VSS	VSS	VSS	VSS
F	VSS	VSS	VSS	VSS
G	PMIC_SWOUT	PMIC_SWOUT	VSS	VSS
H	PMIC_SWIN			RSVD
J	PMIC_BSTOUT			VTT_DDR
K	OTG_VBUS			VDD_DDR
L	PMIC_BSTIN			VREF_DDR
M	PMIC_BSTIN	BYPASS_REG1V8	VSS	VSS
N	VSS	VSS	VSS	VSS
P	RSVD	RSVD		
R	RSVD	RSVD	NJTRST	JTDO-TRACESWO
T	PE6	PD6	PD3	PE3
U	PD7	PD5	PD1	PA9
V	PG15	PD4	PD0	PB7

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Table 5-4 - OSD32MP15x Ball Map Top View (Columns N-T)

	13	14	15	16
A	PB10	PB13	PA2	PA5
B	PH2	PB12	PC1	PA4
C	PH3	PG11	PG5	PA1
D				PG8
E	VSS	VSS	VSS	PE9
F	VSS	VSS	VSS	PD12
G	VSS	VSS	VSS	PF7
H	VSS	VSS	VSS	PF10
J	VSS	VSS	VSS	VSS
K	VSS	VSS	VSS	VSS
L	VSS	VSS	VSS	PA10
M	VSS	VSS	VSS	RSVD
N	VSS	VSS	VSS	DSI_CKP
P				DSI_CKN
R	JTDI	JTMS-SWDIO	JTCK-SWCLK	PC7
T	PB8	PB14	PA15	PC8
U	PB9	PB4	PG6	PC9
V	PB15	PB3	PE5	PC10

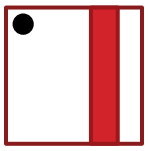

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Table 5-5 - OSD32MP15x Ball Map Top View (Columns U-Y)

	17	18
A	PC0	
B	PA6	PF11
C	PB5	PG10
D	PE7	PE8
E	PE10	PD11
F	PD13	PF6
G	PF8	PF9
H	PG7	PB6
J	USB_DM2	USB_DP2
K	USB_DP1	USB_DM1
L	PA11	PA12
M	PG9	PB2
N	DSI_D1P	DSI_D1N
P	DSI_D0P	DSI_D0N
R	PE4	PC6
T	PA8	PF2
U	PC11	PD2
V	PC12	

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5.1 Ball Description

Table 5-6 lists all the unique signals of the OSD32MP15x and provides the pin number of the OSD32MP15x as well as a mapping to the equivalent pin on the STM32MP1 TFBGA361 package. All the processor signals have the same function as the equivalent pin in the STM32MP1 except where noted.

The OSD32MP15x also provides access to the VREF- signal of the STM32MP15x which is not accessible in the TFBGA361 package.

The functions of each of the pins can be configured through the CubeMX software. For more detail on the pin functions please refer to the datasheet of the integrated device in section 4.1.

Table 5-6 - OSD32MP15x Ball Descriptions

Pin Name	Default Function Description	Pin Number		Notes
		OSD32MP15x	STM32MP15x TFBGA361 Package	
ANA0	Analog Input 0	L1	U3	
ANA1	Analog Input 1	L2	U4	
BOOT0	Boot Pin 0	J6	N1	Internal pull down within MP1 processor. Can use adjacent VDD or VSS ball to configure boot mode. Boot Mode '000' uses the serial port.
BOOT1	Boot Pin 1	H6	N4	
BOOT2	Boot Pin 2	G6	M2	
BYPASS_REG1V8	1V8 Regulator Bypass	M10	AB13	
DSI_CKN	DSI Clock Negative	P16	A16	
DSI_CKP	DSI Clock Positive	N16	B16	
DSI_D0N	DSI Data 0 Negative	P18	B15	
DSI_D0P	DSI Data 0 Positive	P17	C15	
DSI_D1N	DSI Data 1 Negative	N18	A17	
DSI_D1P	DSI Data1 Positive	N17	B17	
EEPROM_WP	EEPROM Write Protect	P4	N/A	*Write Protect Pin for EEPROM. It is internally Pulled Up. Refer to the Passives Section for more information*
HSE_OSC_OEN	High Speed Oscillator Enable	J1	N/A	Enable Pin for the integrated HSE. Refer to the MEMS Oscillators Section for more information
HSE_OSC_TP	High Speed Oscillator Output	J2	P1	Output of HSE That is connected to input for HSE PH0-OSC_IN
JTCK-SWCLK	JTAG Test Clock/Serial Wire Clock	R15	B20	
JTDI	JTAG Data input	R13	A20	
JTDO-TRACESWO	JTAG Test Data Output/Trace Asynchronous Data Out	R12	A19	
JTMS-SWDIO	JTAG Test Mode Select/Serial Wire Data In/Out	R14	C20	
NJTRST	JTAG Test Reset	R11	B19	
NRST	Application Pad Reset Input/ Output	M3	M3	
NRST_CORE	VDD_CORE Reset input	N4	M4	
OTG_VBUS	USB OTG VBUS	K9	AC19	

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PA0/PMIC_INTN	Port A Pin 0	L3	AB3	This pin is connected internally to PMIC INTN
PA1	Port A Pin 1	C16	AA4	
PA10	Port A Pin 10	L16	Y17	
PA11	Port A Pin 11	L17	AA18	
PA12	Port A Pin 12	L18	AB19	
PA13	Port A Pin 13	A3	N2	
PA14	Port A Pin 14	B3	T2	
PA15	Port A Pin 15	T15	C19	
PA2	Port A Pin 2	A15	AC3	
PA3	Port A Pin 3	A5	U2	
PA4	Port A Pin 4	B16	V4	
PA5	Port A Pin 5	A16	V3	
PA6	Port A Pin 6	B17	AC8	
PA7	Port A Pin 7	A12	AB8	
PA8	Port A Pin 8	T17	A13	
PA9	Port A Pin 9	U12	A8	
PB0	Port B Pin 0	A11	AB6	
PB1	Port B Pin 1	B11	AA7	
PB10	Port B Pin 10	A13	Y3	
PB11	Port B Pin 11	A9	AB1	
PB12	Port B Pin 12	B14	AC5	
PB13	Port B Pin 13	A14	AA10	
PB14	Port B Pin 14	T14	C13	
PB15	Port B Pin 15	V13	B12	
PB2	Port B Pin 2	M18	Y16	
PB3	Port B Pin 3	V14	A11	
PB4	Port B Pin 4	U14	B13	
PB5	Port B Pin 5	C17	Y8	
PB6	Port B Pin 6	H18	Y14	
PB7	Port B Pin 7	V12	D11	
PB8	Port B Pin 8	T13	AB10	
PB9	Port B Pin 9	U13	B10	
PC0	Port C Pin 0	A17	AB5	
PC1	Port C Pin 1	B15	AA6	
PC10	Port C Pin 10	V16	D15	
PC11	Port C Pin 11	U17	D16	
PC12	Port C Pin 12	V17	D13	
PC13/PMIC_WAKEUP	Port C Pin 13	D6	K2	This pin is connected internally to PMIC WAKEUP
PC14-OSC32_IN	Port C Pin 14 or LSE Oscillator In	N2	L2	
PC15-OSC32_OUT	Port C Pin 15 or LSE Oscillator Out	N1	L1	
PC2	Port C Pin 2	C7	Y2	
PC3	Port C Pin 3	B6	W2	
PC4	Port C Pin 4	B12	AC7	
PC5	Port C Pin 5	C12	AB7	
PC6	Port C Pin 6	R18	B14	
PC7	Port C Pin 7	R16	B11	
PC8	Port C Pin 8	T16	D18	
PC9	Port C Pin 9	U16	D17	
PD0	Port D Pin 0	V11	B8	
PD1	Port D Pin 1	U11	B9	
PD10	Port D Pin 10	V6	B5	
PD11	Port D Pin 11	E18	AC10	
PD12	Port D Pin 12	F16	Y18	
PD13	Port D Pin 13	F17	AA19	
PD14	Port D Pin 14	C3	L3	
PD15	Port D Pin 15	A2	J2	
PD2	Port D Pin 2	U18	D12	
PD3	Port D Pin 3	T11	D14	
PD4	Port D Pin 4	V10	B6	

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PD5	Port D Pin 5	U10	A7	
PD6	Port D Pin 6	T10	D2	
PD7	Port D Pin 7	U9	D10	
PD8	Port D Pin 8	B2	K3	
PD9	Port D Pin 9	B1	K1	
PDR_ON	VDD Power On Reset Enable	M6	R3	
PDR_ON_CORE	VDD_CORE Power On Reset Enable	L6	T3	
PE0	Port E Pin 0	U7	D6	
PE1	Port E Pin 1	T7	C8	
PE10	Port E Pin 10	E17	Y15	
PE11	Port E Pin 11	V5	A4	
PE12	Port E Pin 12	U5	B4	
PE13	Port E Pin 13	T5	A3	
PE14	Port E Pin 14	V4	C6	
PE15	Port E Pin 15	U4	D3	
PE2	Port E Pin 2	A6	Y1	
PE3	Port E Pin 3	T12	C9	
PE4	Port E Pin 4	R17	D19	
PE5	Port E Pin 5	V15	C11	
PE6	Port E Pin 6	T9	C10	
PE7	Port E Pin 7	D17	AA11	
PE8	Port E Pin 8	D18	AC13	
PE9	Port E Pin 9	E16	AA9	
PF0	Port F Pin 0	U8	D8	
PF1	Port F Pin 1	V8	A5	
PF10	Port F Pin 10	H16	Y12	
PF11	Port F Pin 11	B18	Y10	
PF12	Port F Pin 12	C11	Y9	
PF13	Port F Pin 13	A10	Y5	
PF14	Port F Pin 14	B10	AC4	
PF15	Port F Pin 15	C10	Y4	
PF2	Port F Pin 2	T18	A14	
PF3	Port F Pin 3	C6	U1	
PF4	Port F Pin 4	V7	D9	
PF5	Port F Pin 5	T8	D7	
PF6	Port F Pin 6	F18	AA13	
PF7	Port F Pin 7	G16	AB12	
PF8	Port F Pin 8	G17	AC11	
PF9	Port F Pin 9	G18	AA14	
PG0	Port G Pin 0	C8	AC2	
PG1	Port G Pin 1	B8	W1	
PG10	Port G Pin 10	C18	AB11	
PG11	Port G Pin 11	C14	Y7	
PG12	Port G Pin 12	A4	K4	
PG13	Port G Pin 13	B7	AA2	
PG14	Port G Pin 14	A7	AA1	
PG15	Port G Pin 15	V9	B7	
PG2	Port G Pin 2	A8	V2	
PG3	Port G Pin 3	C9	T4	
PG4	Port G Pin 4	B9	AB2	
PG5	Port G Pin 5	C15	Y6	
PG6	Port G Pin 6	U15	A10	
PG7	Port G Pin 7	H17	AC14	
PG8	Port G Pin 8	D16	AB9	
PG9	Port G Pin 9	M17	Y13	
PH10	Port H Pin 10	U3	C2	
PH11	Port H Pin 11	V2	C4	
PH12	Port H Pin 12	U2	B2	
PH13	Port H Pin 13	U1	D1	
PH14	Port H Pin 14	T1	C3	
PH15	Port H Pin 15	T2	B1	
PH2	Port H Pin 2	B13	AB4	

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PH3	Port H Pin 3	C13	AA3	
PH4	Port H Pin 4	U6	B3	
PH5	Port H Pin 5	T6	A2	
PH6	Port H Pin 6	B5	Y11	
PH7	Port H Pin 7	C5	W4	
PH8	Port H Pin 8	T4	D5	
PH9	Port H Pin 9	V3	C5	
PI0	Port I Pin 0	T3	C1	
PI1	Port I Pin 1	R1	E3	
PI10	Port I Pin 10	B4	T1	
PI11	Port I Pin 11	C4	P4	
PI2	Port I Pin 2	R2	E2	
PI3	Port I Pin 3	R3	E1	
PI4	Port I Pin 4	P1	E4	
PI5	Port I Pin 5	P2	F3	
PI6	Port I Pin 6	P3	F4	
PI7	Port I Pin 7	N3	F2	
PI8	Port I Pin 8	C1	L4	
PI9	Port I Pin 9	C2	H4	
PMIC_BSTIN	Input to PMIC Boost	L8, L9, M8, M9	33	Input to PMIC Boost
PMIC_BSTOUT	Output of PMIC Boost	J9, J8	34	Output of PMIC Boost
PMIC_LDO1	Output of PMIC LDO1	J4	23	Output of PMIC LDO1
PMIC_LDO2	Output of PMIC LDO2	G4	18	Output of PMIC LDO2
PMIC_LDO25IN	Input to PMIC LDO2 and LDO5	G3	19	Input to PMIC LDO2 and LDO5
PMIC_LDO5	Output of PMIC LDO5	G8	20	Output of PMIC LDO5
PMIC_LDO6	Output of PMIC LDO6	H4	21	Output of PMIC LDO6
PMIC_PONKEYN	PMIC PONKEYn	D3	17	PMIC PONKEYn. Internal pullup within PMIC to VIN.
PMIC_SWIN	Input of PMIC PWR_SW	H8, H9	37	Input of PMIC PWR_SW
PMIC_SWOUT	Output of PMIC PWR_SW	G10, G9	38	Output of PMIC PWR_SW
PMIC_VBUSOTG	Output of PMIC PWR_USB_SW	K8	35	Output of PMIC PWR_USB_SW
PMIC_VOUT4	Output of PMIC Buck4	H3, J3	25	Output of PMIC Buck4
PWR_LP	Core supply Low-power Stop mode selection output	K6	N3	
PWR_ON/PMIC_PWR CTRL	Core supply enable output	D5	R2	This pin is connected internally to the PMIC PWRCTRL Pin
PZ0	Port Z Pin 0	F1	G3	
PZ1	Port Z Pin 1	F2	G1	
PZ2	Port Z Pin 2	F3	J4	
PZ3	Port Z Pin 3	E1	G4	
PZ4/PMIC_SCL	Port Z Pin 4	E2	G2	This Pin must be configured as an I2C Bus. It is connected internally to PMIC SCL and EEPROM SCL
PZ5/PMIC_SDA	Port Z Pin 5	E3	H2	This Pin must be configured as an I2C Bus. It is connected internally to PMIC SDA and EEPROM SDA
PZ6	Port Z Pin 6	D1	H1	
PZ7	Port Z Pin 7	D2	J3	
RSVD	RSVD	H12, R9, R10, P9, M16, D9, D8, D7, D10, P10		Reserved for Future Use
USB_DM1	USB Port 1 DM	K18	AB17	
USB_DM2	USB Port 2 DM	J17	AB16	
USB_DP1	USB Port 1 DP	K17	AC17	

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USB_DP2	USB Port 2 DP	J18	AC16	
VBAT	Backup battery supply input	K3	1F1	
VDD_CORE	Test Point for VDD_CORE Voltage	R4	7	Test Point for VDD_CORE Voltage
VDD_DDR	Test Point for VDD_DDR Voltage	K12	11	Test Point for VDD_DDR Voltage
VDD	Main IO and VDD domain supply input	M4, G7, M7, L7, L4, K7, K4, J7, H7	1F3, 1G4, 1H3, 1H5, 1J2, 1J4, 1J6	Pins M4, L4, and K4 should be connected together. Pins M7, L7, J7, H7, and G7 should be connected together. These two groups do not need to be connected together.
VDD1V2_DSI_REG	Test Point for VDD1V2_DSI_REG	R6	C18	Test Point for VDD1V2_DSI_REG
VDD3V3_USB	Test Point for VDD3V3_USB	R5	39	Test Point for VDD3V3_USB
VDDA	Analog domain supply	M1	1H1	
VDDA1V1_REG	Test Point for VDDA1V1_REG	R8	AB15	Test Point for VDDA1V1_REG
VDDA1V8_REG	Test Point for VDDA1V8_REG	R7	AB14	Test Point for VDDA1V8_REG
VIN	Input Power Rail	H2, H1, G2, G1		Input Power Rail for the SiP. Provides power to Buck1, Buck2, Buck3, Buck4 and VIN of the STPMIC1.
VREF_DDR	Test Point for VREF_DDR Voltage	L12	16	Test Point for VREF_DDR Voltage
VREF-	External Reference Voltage for ADC and DAC	K2		VREF- For the STM32MP1. VREF- is not pinned out in the TFBGA361 package but is Ball N6 in the LFBGA448 package
VREF+	External Reference Voltage for ADC and DAC	M2	R4	
VSS	Digital ground power supply	K14, M13, M12, M11, L5, L15, L14, L13, K5, K15, N10, K13, J5, J16, J15, J14, K16, N5, P8, P7, P6, P5, N9, N8, M15, N6, M14, N15, N14, N13, N12, N11, H14, M5, N7, E4, H5, F11, F10, E9, E8, E7, F13, E5, F14, E15, E14, E13, E12, E11, E10, D4, E6, G11, H15, H13, G5, G15, G14, F12, G12, J13, F9, F8, F7, F6, F5, F4, F15, G13	1A3, 1A5, 1A7, 1B2, 1B4, 1B6, 1B8, 1C1, 1C3, 1C5, 1C7, 1C9, 1D2, 1D4, 1D6, 1D8, 1E1, 1E3, 1E5, 1E7, 1E9, 1F2, 1F4, 1F6, 1F8, 1G3, 1G5, 1G7, 1G9, 1H4, 1H6, 1H8, 1J3, 1J5, 1J7, A1, A23, AA12, AA21, AA5, AA8, AC1, AC23, C12, C21, C7, D4, F21, H3, K21, P21, P	
VSSA	Analog ground power supply	K1	1H2	Internally connected to VSS
VTT_DDR	Test Point for VTT_DDR	J12	14	Test Point for VTT_DDR

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5.2 Reserved Balls

The OSD32MP15x ball map contains balls which are marked Reserved. These balls must remain unconnected on the system PCB since they may be used for other purposes in future versions of the OSD32MP15x.

5.3 Test Point Signals

There is a subset of signals that are available on the OSD32MP15x ball map but ***should not be*** used externally to the device unless specified. These signals are used internally to the OSD32MP15x and using them could significantly affect the performance of the device. They are provided for test purposes only. The list of signals that should not be used can be found in Table 5-7.

Table 5-7 – Test Point Signals

Test Point Only Signals
VDD_CORE
VDD_DDR
VDD1V2_DSI_REG
VDD3V3_USB
VDDA1V1_REG
VDDA1V8_REG
VREF_DDR
VTT_DDR

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6 OSD32MP15x Components

The OSD32MP15x integrates the ST Microelectronics STM32MP15x Dual Arm® Cortex®-A7 and Arm® Cortex®-M4 processor along with the ST STPMIC1A PMIC, up to 1 GB of DDR3L Memory, a 4KB EEPROM for non-volatile storage, MEMS Oscillator for the primary clock input, and the resistors, capacitors, and inductors into a single design-in-ready package. The following sections contains any specific device information needed for the integrated components to design your system with the OSD32MP15x. Specifics on the Power Management System will be covered in Section 7.

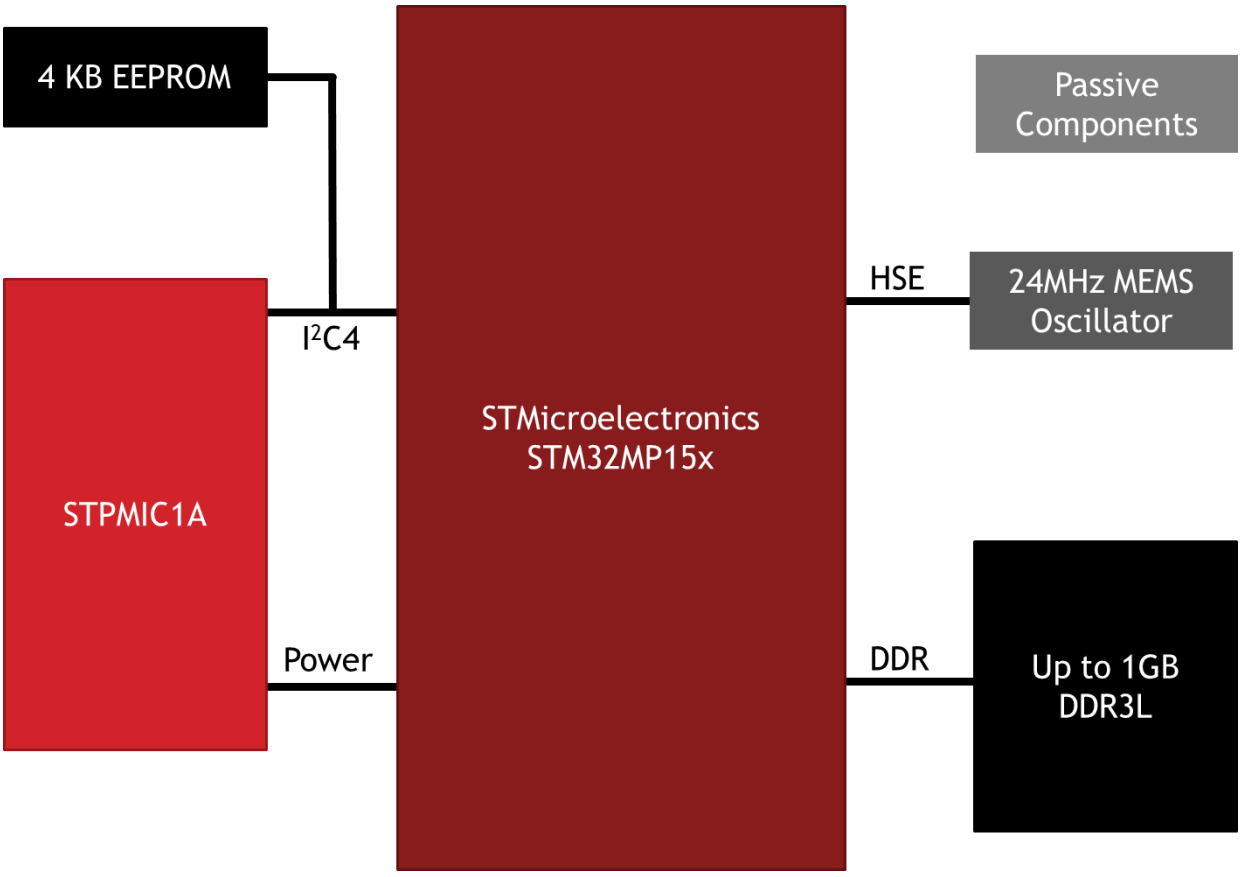

Figure 6.1 - OSD32MP15x Internal Connections Block Diagram

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6.1 STM32MP15x Processor

The heart of the OSD32MP15x is the ST Microelectronics Dual Arm® Cortex®-A7 + Arm® Cortex® M4 STM32MP15x processor. The processor in the OSD32MP15x is configured to perform identically to a standalone device. Please refer to the data sheet in the Reference Documents section for details on using the STM32MP15x processor. Additionally, the different available variants of the STM32MP15x processor can be found in Section 3.

6.1.1 I/O Voltages

The I/O Voltages of the OSD32MP15x range from 1.71V to 3.6V just like the STM32MP15x. This voltage is driven by the VDD internal power rail of the OSD32MP1. To adjust the I/O voltage the VDD internal power rail needs to be set accordingly.

Please refer to the STM32MP15x datasheet and the STM32MP1 Hardware Design Getting Started Guide in the Reference Documents section and the VDD section of this document for more information.

6.2 DDR3L Memory

The OSD32MP15x integrates a DDR3L memory and handles all the connections needed between the STM32MP15x and the DDR3L. You will still have to set the proper registers to configure the STM32MP15x DDRCTRL and DDRPHYC to work correctly with the memory included in the OSD32MP15x. Typically, this would require you to run through the procedure outlined in the ***DDR configuration on STM32MP1 Series MPUs*** in the Reference Documents section of this document.

However, this procedure has been run for all variations of the OSD32MP15x. The recommend values for the DDR register settings can be found in the Octavo Systems github here: https://github.com/octavosystems/osd32mp1-ddr.

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6.3 MEMS Oscillators

The OSD32MP15x integrates a main 24MHz oscillator and is used as the High-speed External (HSE) clock source.

This section outlines the key parameters for the oscillator that is integrated.

6.3.1 HSE MEMS Oscillator

The OSD32MP15x integrates a 24MHz oscillator used as the HSE clock source. The key parameters for the oscillator are outlined in Table 6-1.

Table 6-1 – HSE MEMS Oscillator Parameters

Parameter	Min	Typ	Max	Units	Notes
Active Supply Current		790		µA	
Standby Supply Current		0.7	1.3	µA	
Initial Stability			±15	ppm	@25C
Frequency Stability			±100	ppm	All temp ranges
Aging			±3	ppm	First year @ 25C
Period Jitter, RMS			25	ps_{RMS}	
Cycle-to-Cycle Jitter			2.5	ns	
Frequency		24		MHz	

The pin HSE_OSC_TP is the output of the MEMS Oscillator. This is the same signal that is being fed into the processor.

To disable the HSE Oscillator the HSE_OSC_OEN pin must be pulled high.

Note: The MEMS Oscillator has an integrated weak internal pull down on HSE_OSC_OEN. This enables the oscillator by default. However, it is recommended that designs incorporate a test point at minimum on HSE_OSC_OEN.

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6.4 EEPROM

The OSD32MP15x contains a 4KB EEPROM for non-volatile storage of configuration information. The EEPROM is connected to I2C4 at the 7-bit I2C address 0x50 (0b1010000). Please refer to the data sheet in the Reference Documents section for details on using the EEPROM.

6.4.1 EEPROM Contents

EEPROM address space 0x000 to 0xEFF is empty and can be used for board specific information or other configuration data. The final 256 bytes of the EEPROM (0xF00 to 0xFFF) are reserved for device specific information. The reserved space contents of the EEPROM can be found in Table 6-2

Table 6-2 - EEPROM Contents Programmed by Octavo Systems

Name	Description	Size (bytes)	Start address	End address	Contents
RSVD	Reserved for Future Use	256	0xF00	0xFFF	All 0xFF

6.4.2 EEPROM Write Protection

By default, the EEPROM is write protected (i.e., the EEPROM_WP pin is pulled high, see Table 2-2). To program values into the EEPROM, it is required to drive the EEPROM_WP pin to a logic low. See the OSD32MP15x Layout Guide in the Reference Documents section for layout / manufacturing recommendations for the EEPROM_WP pin.

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7 Power Management

The power management portion of the OSD32MP15x consists of the STPMIC1A (PMIC). The PMIC provides the necessary power rails to the STM32MP15x, DDR3L, EEPROM and all the other internal components to the OSD32MP15x. It also provides power supply outputs that may be used to power circuitry external to the OSD32MP15x. The PMIC is connected to I2C4 at the 7-bit I2C address 0x33 (0b0110011). This section describes how to power the OSD32MP15x in a system and the outputs that can be used.

7.1 Power Block Diagram

Figure 7.1 shows the power block diagram of OSD32MP15x describing the power connections inside the SiP. Please note that passive components are not shown.

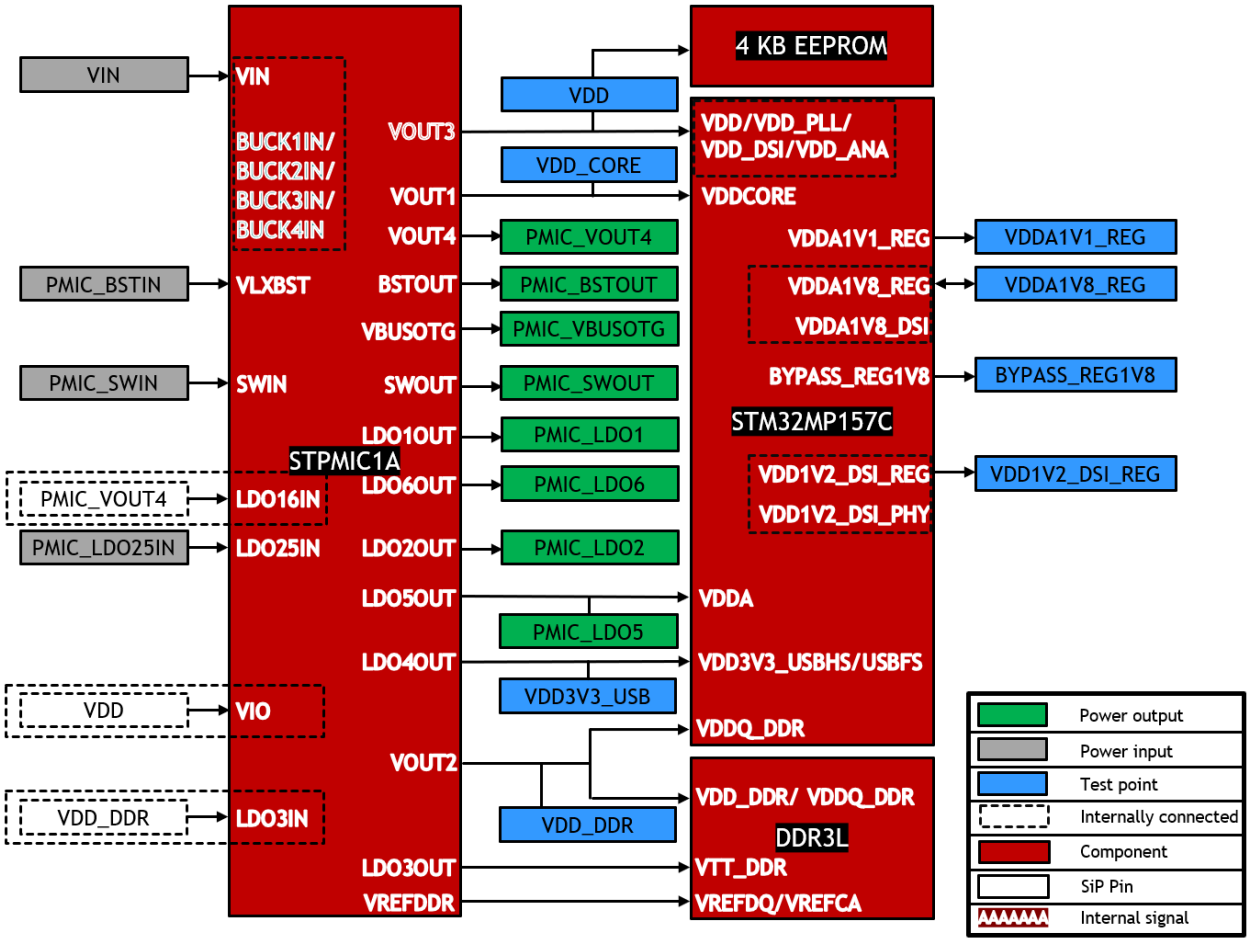

Figure 7.1 - OSD32MP15x Power Block Diagram

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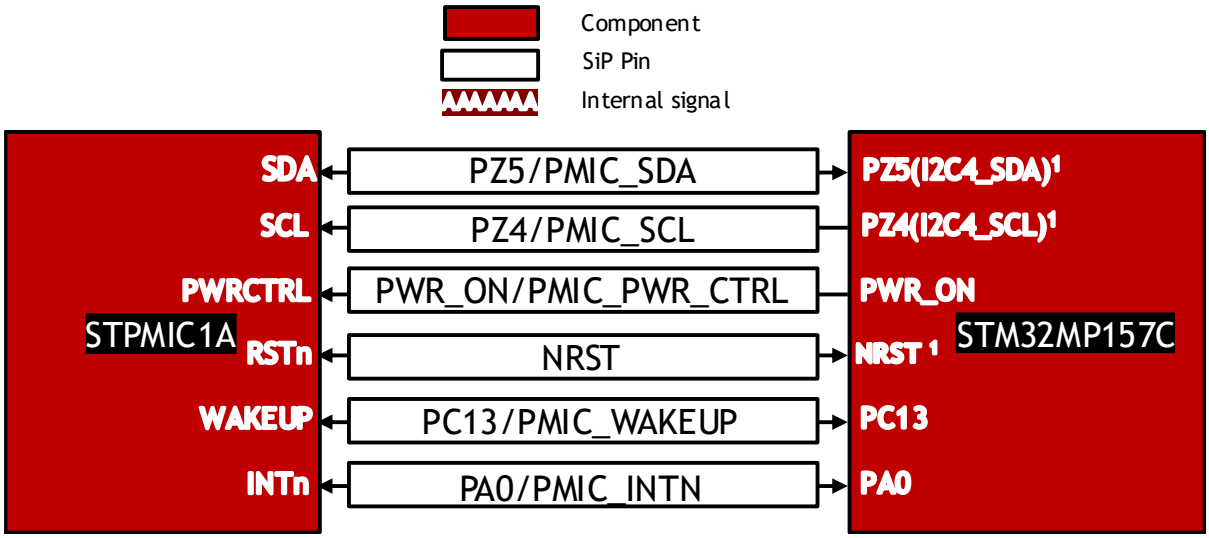
7.2 Interface between STM32MP15x and STPMIC1A

The PMIC and the processor can interact through a set of control and communication signals that form the interface between them. Figure 7.2 shows the interface signals between STM32MP15x and STPMIC1A.



(1) These pins are internally pulled up to VDD

Figure 7.2: OSD32MP15x STPMIC1A-STM32MP15x Interface Diagram

7.3 Power Input

OSD32MP15x has two power inputs. VIN is the main power input and VBAT is the backup battery power input.

7.3.1 VIN Power Input

The OSD32MP15x is powered by VIN on the STPMIC1A. This input supports a voltage range from 2.8V to 5.5V that is suitable for applications that are powered by 5V DC wall adaptors, 1S Li-Ion/Li-PO Battery (nominally 3.7V), or from a USB port.

While the device supports operating voltage ranges from 2.8V to 5.5V, by default a voltage of at least 3.5V is required for the device to enter the POWER_ON state. This can be adjusted by modifying the VIN_{OK_Rise} threshold in the STPMIC1A Non-Volatile Memory. For instruction on modifying this value please see the STPMIC1 Non-Volatile Memory Programming Guide and the STPMIC1A datasheet found in the Reference Documents section of this document.

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7.3.2 VBAT Power Input

VBAT input of OSD32MP15x provides access to VBAT pin of STM32MP15x. This input powers the Backup domain consisting of RTC, backup registers, the retention RAM and the backup SRAM in VBAT mode when Power-Down-Reset (PDR) supervisor detects that VDD has dropped below PDR level. This input can be provided using an external battery or a supercapacitor and supports a voltage range from 1.2V to 3.6V. If no external battery is used, this pin must be connected to VDD.

7.4 Optional power inputs

OSD32MP15x has three optional power inputs that can power external component. They are described below.

7.4.1 PMIC_BSTIN Power Input

PMIC_BSTIN of OSD32MP15x provides access to BSTIN pin of STPMIC1A. This input powers the Boost converter of STPMIC1A. This input supports a voltage range from 3.3V to 5.5V. In addition to the output, the boost converter powers a power switch that supplies PWR_USB_SW inside STPMIC1A connected to the output pin PMIC_VBUSOTG.

7.4.2 PMIC_SWIN Power Input

PMIC_SWIN of OSD32MP15x provides access to SWIN of STPMIC1A. This input supplies the power switch PWR_SW of STPMIC1A, which outputs to pin PMIC_SWOUT.

7.4.3 PMIC_LDO25IN

PMIC_LDO25IN of OSD32MP15x provides access to LDO25IN of STPMIC1A. This input powers LDOs 2 and 5 of STPMIC1A. The outputs of these LDOs are described in the Power Output section

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7.5 Power Output

The OSD32MP15x produces the following output power supplies that can be used for general system power. Each of the output voltages can be programed by the STM32MP15x processor via the I2C bus. Each of the power supplies has a default output voltage and rank as specified in the STPMIC1A column of Table 1 of the STPMIC1 datasheet. The non-volatile memory (NVM) of the PMIC can be set to change the default output voltage and rank of the power supplies. By default, the final power configuration is set in the Device Tree during boot.

When changing the output voltage of any of the power outputs listed below, all power dependencies must be comprehended, and each power input must have enough input voltage and input current. For example, the power input for PMIC_LDO1 and PMIC_LDO6 is internally connected to PMIC_VOUT4 power output. Each of the LDOs has a maximum dropout voltage of 300mV. Therefore, to set either of the LDOs to 3.3V, PMIC_VOUT4 must also be set to 3.6V. Please refer to the Power Block Diagram to understand which power inputs and outputs are connected within the OSD32MP15x.

Please refer to the datasheet for the STPMIC1A and the STMP32MP15x in the Reference Documents section for more information.

7.5.1 PMIC_VOUT4

PMIC_VOUT4 is produced by Buck4 of the STPMIC1A. The input of Buck4 is tied to the VIN pin of the OSD32MP15x. By default, it is configured to operate at 3.3V and will start automatically 10ms after a “Turn_ON” condition. It can be programmed to have a voltage output from 0.6V to 3.9V.

7.5.2 PMIC_LDO1

PMIC_LDO1 is produced by LDO1 of the STPMIC1A. The input of LDO1 is tied to PMIC_VOUT4 (Buck4 Output) internal to the OSD32MP15x. By default, LDO1 is configured to operate at 1.8V and will not start automatically. It can be programmed to have a voltage output from 1.7V to 3.3V.

Note that PMIC_LDO1 and PMIC_LDO6 are powered by PMIC_VOUT4. The total load on these LDOs plus any external load on PMIC_VOUT4 must not exceed the capabilities of the Buck4 regulator outlined in Section 8.

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7.5.3 PMIC_LDO2

PMIC_LDO2 is produced by LDO2 of the STPMIC1A. The input of LDO2 is brought out to the PMIC_LDO25IN pin. By default, LDO2 is configured to operate at 1.8V and will not start automatically. It can be programmed to have a voltage output from 1.7V to 3.3V.

In order to use PMIC_LDO2 or PMIC_LDO5, the PMIC_LDO25IN pin must be connected to a power output that can supply the required voltage and current for both LDOs.

7.5.4 PMIC_LDO5

PMIC_LDO5 is produced by LDO5 of the STPMIC1A. The input of LDO is brought out to the PMIC_LDO25IN pin. By default, LDO5 is configured to operate at 2.9V and will start automatically 10ms after a “Turn_ON” condition. It can be programmed to have a voltage output from 1.7V to 3.3V

The PMIC_LDO5 output is internally connected to VDDA power input pin of STM32MP15x. This input powers the Analog domain (ADC/DAC/VREFBUF) of the STM32MP15x processor.

In order to use PMIC_LDO2 or PMIC_LDO5, the PMIC_LDO25IN pin must be connected to a power output that can supply the required voltage and current for both LDOs.

7.5.5 PMIC_LDO6

PMIC_LDO6 is produced by LDO6 of the STPMIC1A. The input of LDO6 is tied to PMIC_VOUT4 (Buck4 Output) internal to the OSD32MP15x. By default, LDO6 is configured to operate at 1.0V and will not start automatically. It can be programmed to have a voltage output from 0.9V to 3.3V.

Note that PMIC_LDO1 and PMIC_LDO6 are powered by PMIC_VOUT4. The total load on these LDOs plus any external load on PMIC_VOUT4 must not exceed the capabilities of the Buck4 regulator outlined in Section 8.

7.5.6 PMIC_BSTOUT

PMIC_BSTOUT is the output of the integrated Boost converter in the STPMIC1A. The input to the Boost converter is brought out to the PMIC_BSTIN pin. The OSD32MP15x also integrates an input inductor and capacitor so only a voltage input needs to be provided to use the boost converter (i.e. PMIC_BSTIN is not directly connected to VLXBST).

The Boost converter has a fixed output voltage of 5.2V and is designed to power USB devices. It also supports the BYPASS mode as described in the STPMIC datasheet.

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7.5.7 PMIC_VBUSOTG

PMIC_VBUSOTG is the output of the PWR_USB_SW in the STPMIC1A. It is designed to power USB OTG port or USB Type-C. The input of the switch is connected to the PMIC_BSTOUT internal to the STPMIC1A. The output voltage of the PWR_USB_SW is approximately equal to the PMIC_BSTOUT.

7.5.8 PMIC_SWOUT

PMIC_SWOUT is the output of the PWR_SW internal to the STPMIC1A. The input of the switch is brought out to the PMIC_SWIN pin. The output voltage of PMIC_SWOUT will be about equal to the input voltage provided on PMIC_SWIN.

7.6 Internal Power

The OSD32MP15x has power rails generated by the STPMIC1A that are used internally by the OSD32MP15x. While some of the output voltages of the regulators can be adjusted, they should not be adjusted. Adjusting the voltages on these rails will cause the OSD32MP15x device not to function.

These power pins should not be uses to power external components. Doing so can prevent the OSD32MP15x from functioning properly. However, they may be used for debugging / monitoring the system and as reference voltage outputs.

7.6.1 VDD_CORE

VDD_CORE is generated by Buck1 in the STPMIC1A. It provides the core power to the STM32MP15x integrated into the OSD32MP15x. By default, its voltage is 1.2V. See Table 7-1 for required STPMIC1A configuration of this voltage rail.

7.6.2 VDD_DDR

VDD_DDR is generated by Buck2 in the STPMIC1A. It provides the power to the DDR memory integrated into the OSD32MP15x. By default, its voltage is 1.1V. See Table 7-1 for required STPMIC1A configuration of this voltage rail.

7.6.3 VDD

VDD is generated by Buck3 in the STPMIC1A. It provides the power to the VDD Power domain of the STM32MP15x integrated into the OSD32MP15x. By default, this voltage is set to 3.3V.

The VDD output is used to set the I/O voltage for the STM32MP15x. Therefore, the output voltage can be modified to support both 1.8V and 3.3V I/O operation.

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The VDD Pins are separated into two (2) logical groups in the ball map. Each pin in the respective group must be connected to the other pins in that same group. The two groups do not need to be connected to each other. Specifically Pins M4, L4, and K4 must be connected together and Pins M7, L7, K7, J7, H7, and G7 must be connected together.

7.6.4 VTT_DDR

VTT_DDR is generated by LDO3 in the STPMIC1A. It provides power to the DDR VTT. By default, its voltage is 1.8V. See Table 7-1 for required STPMIC1A configuration of this voltage rail.

7.6.5 VDD3V3_USB

VDD3V3_USB is generated by LDO4 in the STPMI1A. It provides power for the VDD_USB power domain of the STM32MP15x. By default, its voltage is 3.3V. See Table 7-1 for required STPMIC1A configuration of this voltage rail.

7.6.6 VREF_DDR

VREF_DDR is generated by VREFDDR in the STPMI1A. It provides power for the reference voltage for the integrated DDR. By default, its voltage is 0.55V. See Table 7-1 for required STPMIC1A configuration of this voltage rail.

7.6.7 VDD1V2_DSI_REG

VDD1V2_DSI_REG is generated by the $V_{DDA1V2_DSI_REG}$ regulator in the STM32MP15x. It is connected internally within the OSD32MP15x to VDD1V2_DSI_PHY. Its voltage is 1.2V.

7.6.8 VDDA1V1_REG

VDDA1V1_REG is generated by the V_{DDA1V1_REG} regulator in the STM32MP15x. Its voltage is 1.1V.

7.6.9 VDDA1V8_REG

VDDA1V8_REG is generated by the V_{DDA1V8_REG} regulator in the STM32MP15x. It is connected internally within the OSD32MP15x to VDDA1V8_DSI. Its voltage is 1.8V.

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7.6.10 VDDA

VDDA is generated by LDO5 in the STPMIC1A. It provides power to the Analog domain (ADC, DAC, VREFBUF). It can be used as a reference for VREF+. Please refer to STM32MP15x data sheet in the Reference Documents section for a detailed voltage setting range on VDDA power rail.

7.6.11 STPMIC1A Voltage Requirements for OSD32MP15x

The following table shows the required voltage output configuration of STPMIC1A for OSD32MP15x family. These internal voltage rails must be set to required voltages for the devices to function according to specifications.

Table 7-1: STPMIC1A voltage output requirements for OSD32MP15x

STPMIC1A Voltage Rail	OSD32MP15x Pin Name	Voltage Required (V)
LDO3OUT	**VTT_DDR**	0.675V
LDO4OUT	**VDD3V3_USB**	3.3V (Default)
VREFDDR	**VREF_DDR**	0.65V
VOUT1	**VDD_CORE**	1.2V (Default)
VOUT2	**VDD_DDR**	1.35V

7.7 Total Current Consideration

The total current consumption of all power rails must not exceed the recommended input currents described in Table 8-2. This includes power consumption within the SiP from the STM32MP15x, the DDR3L, MEMS Oscillator, and other internal components as well as all external loads on the output power rails from Section 7.5.

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8 Electrical & Thermal Characteristics

Table 8.1 lists electrical and thermal characteristic parameters of OSD32MP15x.

Table 8-1. OSD32MP15x Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted) (1) (2)

			Value	Unit
Supply voltage range (with respect to VSS)	VIN		-0.5 to 6	V
	PMIC_BST_IN		-0.5 to 6	V
	VIN_BAT		-0.3 to 3.9	V
Input/Output voltage range (with respect to VSS)	All pins unless specified separately		-0.3 to 3.6	V
T_C Operating case temperature(3)	Commercial	(B)	0 to 85	°C
	Industrial	(I)	-40 to 85	°C
	Extended	(E)	-20 to 85	°C
T_{stg} Storage temperature			-40 to 125	°C
ESD rating	(HBM) Human body model		±1000	V
	(CDM) Charged device model		±500	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) See the OSD32MP1 Thermal Application Note in the Reference Documents section for more details on measuring case temperature.

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Table 8-2. Recommended Operating Conditions over operating free-air temperature range (unless otherwise noted)

	Min	Nom	Max	Unit
Supply voltage, VIN	3.4		5.5	V
Input current, VIN(4)			2000	mA
Supply voltage, VIN_BAT	1.4		3.6	V
Input current, VIN_BAT			2	mA
Supply voltage, SWIN	4.5		5.5	V
Input current, SWIN			250	mA
Supply voltage, PMIC_BSTIN	3.5		5.5	V
Output voltage range, PMIC_VOUT4	0.6	3.3	3.9	V
Output voltage range, PMIC_LDO1	1.7	1.8	3.3	V
Output voltage range, PMIC_LDO2	1.7	1.8	3.3	V
Output voltage range, PMIC_LDO5	1.7	2.9	3.9	V
Output voltage range, PMIC_LDO6	0.9	1.0	3.3	V
Output voltage range, PMIC_BSTOUT		5.2		V
Output voltage range, PMIC_VBUSOTG		~PMIC_BSTOUT		V
Output voltage range, PMIC_SWOUT		~PMIC_SWIN		V
Output voltage range, VDD_CORE[1]		1.2		V
Output voltage range, VDD_DDR[1]		1.35		V
Output voltage range, VDD[3]		3.3		V
Output voltage range, VTT_DDR[1]		1.8		V
Output voltage range, VDD3V3_USB[1]		3.3		V
Output voltage range, VREF_DDR[1]		0.675		V
Output voltage range, VDD1V2_DSI_REG[1]		1.2		V
Output voltage range, VDDA1V1_REG[1]		1.1		V
Output voltage range, VDDA1V8_REG[1]		1.8		V
Output current, PMIC_VOUT4[2]	0		2000	mA
Output current, PMIC_LDO1 [2]	0		350	mA
Output current, PMIC_LDO2 [2]	0		350	mA
Output current, PMIC_LDO5 [2]	0		350	mA
Output current, PMIC_LDO6 [2]	0		150	mA
Output current, PMIC_BSTOUT [2]	0		500	mA
Output current, PMIC_VBUSOTG [2]	0		500	mA
Output current, PMIC_SWOUT [2]	0		250	mA

(1) *These voltage rails are for reference only and should not be used to power anything on the PCB.*
(2) *Please note that the total input current on VIN must not exceed the recommended maximum value even if individual currents drawn from these power supply outputs are less than or equal to the maximum recommended operating output currents. See section 7.7 for more details.*
(3) *The VDD rail should not be used to power external active components. Low-current passive components, such as pull-up resistors, is acceptable.*
(4) *Supply Voltage must be ≥4V to support the full 2000mA.*

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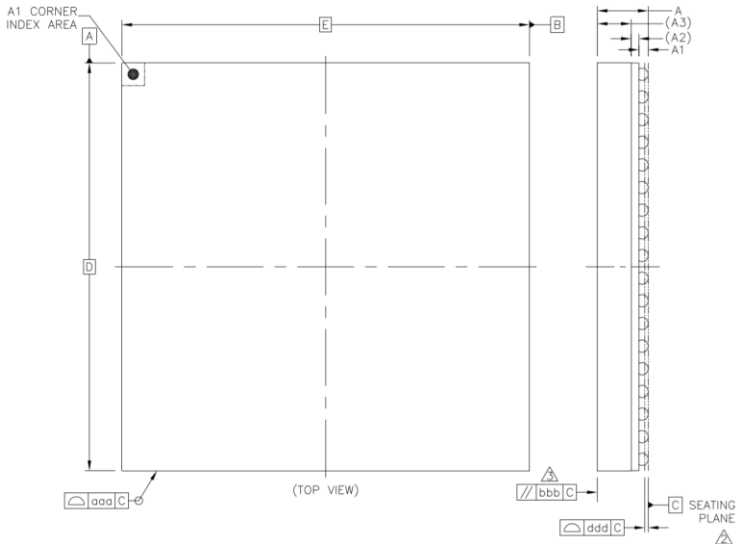
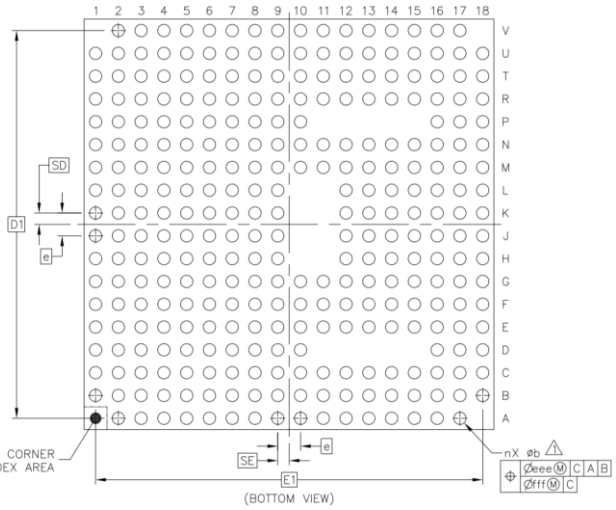
9 Packaging Information

The OSD32MP15x is packaged in a 302 ball, Ball Grid Array (BGA). The package size is 18 X 18 millimeters with a ball pitch of 1 millimeter. This section will give you the specifics on the package.

9.1 Mechanical Dimensions

The mechanical drawings of the OSD32MP15x show pin A1 in the lower left-hand corner when looking at the balls from the bottom of the device.





	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	2.4
STAND OFF	A1	0.36	---	0.46
SUBSTRATE THICKNESS	A2		0.34	REF
MOLD THICKNESS	A3		1.5	REF
BODY SIZE	D		18	BSC
	E		18	BSC
BALL DIAMETER			0.5	
BALL OPENING			0.4	
BALL WIDTH	b	0.44	---	0.64
BALL PITCH	e		1	BSC
BALL COUNT	n		302	
EDGE BALL CENTER TO CENTER	D1		17	BSC
	E1		17	BSC
BODY CENTER TO CONTACT BALL	SD		0.5	BSC
	SE		0.5	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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9.1.1 Landing Pad Sizing

For the nominal ball diameter of 0.50mm, specification IPC-7351A states that for NSMD pads, the nominal land diameter is 0.40mm with a land variation of 0.45mm to 0.35mm. Footprints provided by Octavo Systems generally use the minimum land pad size to enable lower cost routing (see Layout Guide in the Reference Documents section for more information). However, some applications may require a larger land pad size to enable a more robust structural connection to the circuit board or for other manufacturing constraints. Check the requirements of the application and manufacturer to determine the appropriate land pad size.

9.2 Reflow Instructions

The reflow profile for this package should be in accordance with the Lead-free process for BGA. A peak reflow temperature is recommended to be 245°C.

ST Microelectronics provides a good overview of Handling & Process Recommendations in AN2639 for this type of device. A link to the document can be found in the Reference Documents section of this document.

9.3 Storage Requirements

The OSD32MP15x Family of devices are sensitive to moisture and need to be handled in specific ways to ensure they function properly during and after the manufacturing process. The OSD32MP15x Family of devices are rated with a **Moisture Sensitivity Level (MSL) of 4**. This means that they are stored in a sealed Dry Pack with a desiccant bag and a Humidity Indicator Card (HIC). **If the HIC reads > 10% when read at 23 ± 5 C or the HIC is not present; the devices must be baked in per the directions in 9.3.3 before use.**

9.3.1 Floor Life

Once the sealed Dry Pack is opened the OSD32MP15x can be stored **for up to 72 hours in a room ≤ 30°C and ≤60% Relative Humidity (RH). If any of these conditions are not met the devices must be baked as outlined in section 9.3.3 before use.**

9.3.2 Shelf Life

Octavo System devices are shipped in Moisture Barrier Bags (MBB) that have been partially vacuum-sealed with a desiccant bag. This combination supports a shelf life of the devices in an unopened factory bag for **24 Months from the seal date.** If this is exceeded, then the devices must be **baked per the directions in section 9.3.3 before use**.

9.3.3 Baking

The devices need to be baked if they have been exposed to environments outside of the guidelines outlined in sections 9.3.1 and 9.3.2, or if there is concern about the moisture content of the devices. The devices must be baked for **34hrs at 125°C with a RH of <5%.**

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