All the Octavo patches to the device trees now get applied without any issues.

The problem arises when the device tree compiler (dtc), does the compilation after the kernel finishes its build.

The issue is the following:

In the Octavo .dts the following is included:

&i2c4{

    u-boot,dm-pre-reloc;

    pinctrl-names = "default", "sleep";

    pinctrl-0 = <&i2c4\_pins\_z\_mx>;

    pinctrl-1 = <&i2c4\_sleep\_pins\_z\_mx>;

    status = "okay";

    i2c-scl-rising-time-ns = <185>;

    i2c-scl-falling-time-ns = <20>;

    clock-frequency = <400000>;

    /delete-property/ dmas;

    /delete-property/ dma-names;

    pmic:stpmic@33{

        compatible = "st,stpmic1";

        reg = <0x33>;

        interrupts-extended = <&**exti\_pwr** 55 IRQ\_TYPE\_EDGE\_FALLING>;

        interrupt-controller;

        #interrupt-cells = <2>;

        status = "okay";

On kernel version 5.10 and 5.15.24, the node exti\_pwr is defined in file stm32mp151.dtsi

+          exti: interrupt-controller@5000d000 {

+                  compatible = "st,stm32mp1-exti", "syscon";

+                  interrupt-controller;

+                  #interrupt-cells = <2>;

+                  reg = <0x5000d000 0x400>;

+

+                  /\* exti\_pwr is an extra interrupt controller used for

+                  \* EXTI 55 to 60. It's mapped on pwr interrupt

+                  \* controller.

+                  \*/

+                  **exti\_pwr**: **exti-pwr** {

+                         interrupt-controller;

+                         #interrupt-cells = <2>;

+                         interrupt-parent = <&pwr\_irq>;

+                         st,irq-number = <6>;

+                  };

+          };

However, on kernel version 5.15.67, that node doesn’t exist anymore.

It seems the driver for the pmic got some upgrades and now the syntax or details for it should be written a bit different in the device tree.

Now in the same file stm32mp151.dtsi, we see something different:

exti: interrupt-controller@5000d000 {

        compatible = "st,stm32mp1-exti", "syscon";

        interrupt-controller;

        #interrupt-cells = <2>;

        #address-cells = <0>;

        reg = <0x5000d000 0x400>;

        hwlocks = <&hsem 1 1>;

        wakeup-parent = <&pwr\_irq>;

        exti-interrupt-map {

                #address-cells = <0>;

                #interrupt-cells = <2>;

                interrupt-map-mask = <0xffffffff 0>;

                interrupt-map =

                        <0  0 &intc GIC\_SPI 6   IRQ\_TYPE\_LEVEL\_HIGH>,

                        <1  0 &intc GIC\_SPI 7   IRQ\_TYPE\_LEVEL\_HIGH>,

                        <2  0 &intc GIC\_SPI 8   IRQ\_TYPE\_LEVEL\_HIGH>,

                        <3  0 &intc GIC\_SPI 9   IRQ\_TYPE\_LEVEL\_HIGH>,

                        <4  0 &intc GIC\_SPI 10  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <5  0 &intc GIC\_SPI 23  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <6  0 &intc GIC\_SPI 64  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <7  0 &intc GIC\_SPI 65  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <8  0 &intc GIC\_SPI 66  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <9  0 &intc GIC\_SPI 67  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <10 0 &intc GIC\_SPI 40  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <11 0 &intc GIC\_SPI 42  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <12 0 &intc GIC\_SPI 76  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <13 0 &intc GIC\_SPI 77  IRQ\_TYPE\_LEVEL\_HIGH>,

...

                        <32 0 &intc GIC\_SPI 82  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <33 0 &intc GIC\_SPI 83  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <43 0 &intc GIC\_SPI 75  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <44 0 &intc GIC\_SPI 98  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <47 0 &intc GIC\_SPI 93  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <48 0 &intc GIC\_SPI 138 IRQ\_TYPE\_LEVEL\_HIGH>,

                        <50 0 &intc GIC\_SPI 139 IRQ\_TYPE\_LEVEL\_HIGH>,

                        <52 0 &intc GIC\_SPI 140 IRQ\_TYPE\_LEVEL\_HIGH>,

                        <53 0 &intc GIC\_SPI 141 IRQ\_TYPE\_LEVEL\_HIGH>,

                        <54 0 &intc GIC\_SPI 135 IRQ\_TYPE\_LEVEL\_HIGH>,

                        <55 0 &pwr\_irq 0 IRQ\_TYPE\_EDGE\_FALLING 0>,

                        <56 0 &pwr\_irq 1 IRQ\_TYPE\_EDGE\_FALLING 0>,

                        <57 0 &pwr\_irq 2 IRQ\_TYPE\_EDGE\_FALLING 0>,

                        <58 0 &pwr\_irq 3 IRQ\_TYPE\_EDGE\_FALLING 0>,

                        <59 0 &pwr\_irq 4 IRQ\_TYPE\_EDGE\_FALLING 0>,

                        <60 0 &pwr\_irq 5 IRQ\_TYPE\_EDGE\_FALLING 0>,

                        <61 0 &intc GIC\_SPI 100 IRQ\_TYPE\_LEVEL\_HIGH>,

                        <65 0 &intc GIC\_SPI 144 IRQ\_TYPE\_LEVEL\_HIGH>,

                        <68 0 &intc GIC\_SPI 143 IRQ\_TYPE\_LEVEL\_HIGH>,

                        <69 0 &intc GIC\_SPI 94  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <70 0 &intc GIC\_SPI 62  IRQ\_TYPE\_LEVEL\_HIGH>,

                        <73 0 &intc GIC\_SPI 129 IRQ\_TYPE\_LEVEL\_HIGH>;

        };

};

Please advise on how proceed.