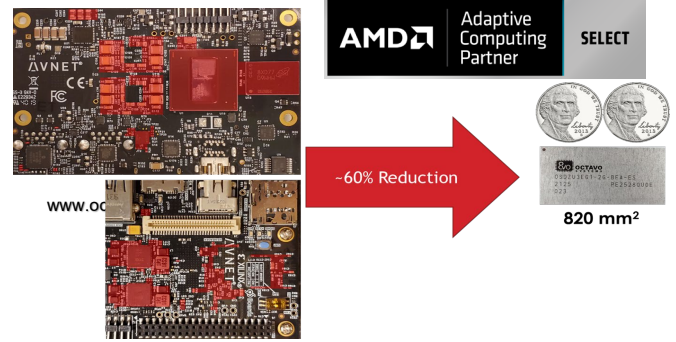


OSDZU3 System-In-Package Family Performance and Flexibility Without the Complexity

The OSDZU3 is the fastest and most flexible way to develop a system around the AMD Zynq UltraScale+ MPSoC. Integrating the XCZU3, LPDDR4 memory, Power Management and other required components into a single package removes the complexity commonly associated with FPGA design. The flexible integration enables the OSDZU3 to use less than half the space of a discrete solution while providing access to all I/O, choice in the I/O voltages, and ability to take advantage of all the power modes of the ZU3.

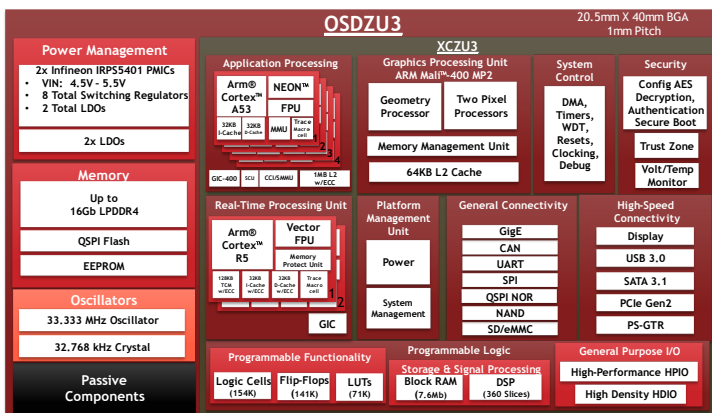
Benefits

- ▶ **Quicker Designs:**
The OSDZU3 provides a known good starting point eliminating traditional design complexities such as DDR layout and Power Management integration. Enabling you to get to market faster or spend more time differentiating your design.
- ▶ **~60% Reduction in Board Area:**
Integrating over 100 components into a single BGA by leveraging IC manufacturing technology enables us to provide a complete system solution in the smallest possible footprint.
- ▶ **Lower Total Cost of Ownership:**
Using a SiP reduces engineering design time by up to 9 months, lowers your PCB and assembly costs, simplifies your supply chain, and provides you a more reliable system. These advantages provide a lower total cost of ownership than a discrete system.
- ▶ **World Class Support:**
Access reference designs, application notes, and an active community on octavosystems.com. We also offer services to review schematics and layout to maximize first pass design success.



Technical Specs

- ▶ Integrated into a 40mm X 20.5mm BGA Package:
 - ▷ ZU3 Zynq UltraScale+ MPSoC
 - ▷ up to 2GB LPDDR4
 - ▷ 2x Infineon IRPS5401 PMICs, 2x LDOs
 - ▷ EEPROM, QSPI
 - ▷ 1x Oscillator, 1x Crystal Oscillator
 - ▷ Passives
- ▶ ZU3 MPSoC Features:
 - ▷ 4x Arm® Cortex®-A53 up to 1.2GHz
 - ▷ 2x Arm® Cortex®-R5F up to 500MHz
 - ▷ Arm® Mali®-400 Based GPU
 - ▷ 16nM FinFET+ Programmable Logic
- ▶ Access to All ZU3 Peripherals Including:
 - ▷ PCIe® Gen2 x4
 - ▷ 2x USB 3.0
 - ▷ SATA 3.1
 - ▷ Display Port
 - ▷ 4x Ethernet 10/100/1000
 - ▷ 2x USB 2.0
 - ▷ 2X SD/SDIO, 2x UART, 2x CAN2.0B
 - ▷ 2x I2C, 2x SPI
 - ▷ 78x MIO
- ▶ Complete Access to UltraScale Programmable Logic:
 - ▷ 154K System Logic Cells
 - ▷ 7.6 Mb Block RAM
 - ▷ 360 DSP Slices
 - ▷ 96 HD I/O, 156 HP I/O
- ▶ Package Options:
 - ▷ 40mm X 20.5mm (1.58in X 0.81in) 600 Ball BGA
 - ▷ 1mm BGA spacing
- ▶ Power:
 - ▷ IN: 4.5V – 5.5V
 - ▷ OUT: 2x Programmable Buck
 - ▷ Flexible I/O voltages
 - ▷ Ability to leverage Low Power modes with control of individual domains.



https://octavosystems.com/octavo_products/osdzu3/

Ordering Information

Now in full production. Please contact your Local Avnet, AMD, or Octavo Systems Representative for more information on device options.

Part Number	AMD MPSoC	A53 Cores	A53 Speed (MHZ)	R5F Cores	3D GPU	QSPI	LPDDR4	Package	Temp Range	QSPI Voltage
OSDZU3EG1-2G-BFA	ZU3EG-1	4	1200	2	X	32MB	2GB	40mm x 20.5mm	0° to 85° C	3.3V
OSDZU3EG1-2G-IFA									-40° to 85° C	
OSDZU3EG1-2G-HFA									-40° to 100° C	
OSDZU3EG1-2G-BFB									0° to 85° C	1.8V
OSDZU3EG1-2G-IFB									-40° to 85° C	
OSDZU3EG1-2G-HFB									-40° to 100° C	

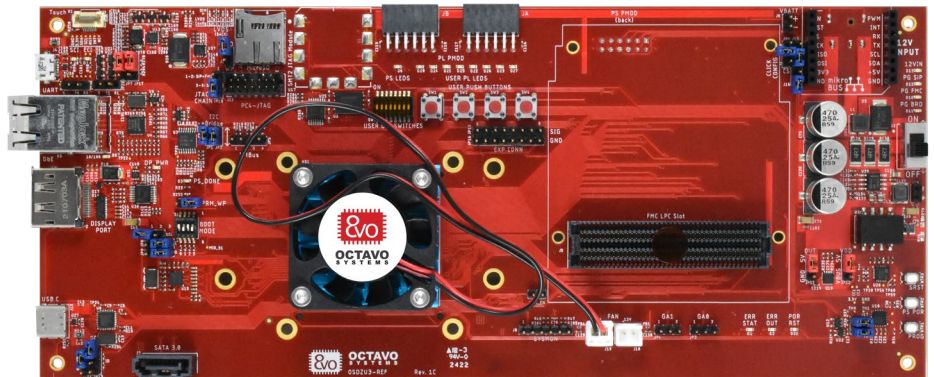
Development Tools

OSDZU3-REF Development Platform

Powerful Prototyping Platform

The OSDZU3-REF is a powerful prototyping platform that provides access to the most common peripherals and has a number of expansion options including FMC, PMOD, and Click connectors. This platform is based on the [UltraZed PCIe Carrier Card](#) from Avnet.

- ▶ Features OSDZU3 device on board
- ▶ Key Interfaces:
 - ▷ USB-C
 - ▷ SATA Host
 - ▷ FMC Low Pin Connector
 - ▷ 3x PMOD
 - ▷ Display Port
 - ▷ LVDS Display + Touch
 - ▷ 1Gb Ethernet
- ▶ 4 Layer Single Board Design
- ▶ Completely Open-Source Design
- ▶ Available Now



Software Support

The OSDZU3 family of System-in-Package Devices are compatible with all software and tools for the ZU3 MPSoC. It can be integrated into Vivado and Vitis. Octavo Systems also provides a PetaLinux build developed in conjunction with [DesignLinx](#).

