OSD335x-SM Overview

Rev. 1 4/28/2017

Introduction

The OSD335x-SM is the smallest System-In-Package (SiP) device in the OSD335x Family. At 21mm X 21mm, it is 40% smaller than the OSD335x and 60% smaller than the equivalent discrete system. The OSD335x-SM integrates all the core components in the OSD335x, including the TI Sitara ARM® Cortex®-A8 AM335x processor, DDR3 memory, TL5209 LDO, TPS65217C PMIC, all the needed passives, and adds 4KB of EEPROM.

The OSD335x-SM also gives designers more flexibility while making it easier to layout their system. A new optimized Pin Map allows single layer escaping of all the BGA pins. The I/O and ADC voltages are programable and there is also more control over the PMIC.

The OSD335x-SM is the perfect solution for the designer that is looking for the most flexible ARM-based solution in the smallest footprint.

Features

- TI AM335x, TPS65217C, TL5209, DDR3, 4KB EEPROM and needed Passive components integrated into a single package
- TI AM335x Features:
  - ARM® Cortex®-A8 up to 1GHz
  - 8 channel 12-bit SAR ADC
  - Dual Ethernet 10/100/1000
  - Dual USB 2.0 HS OTG + PHY
  - MMC, SD and SDIO x2
- Access to All AM335x GPIOs and Peripherals
- Up to 1GB DDR3
- Optimized Pin Map
- Configurable I/O Voltages/ADC Range

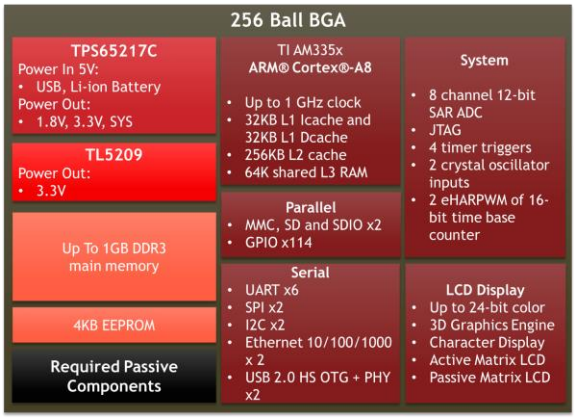


Figure 1. OSD335x-SM Block Diagram

- Access to PMIC Mux In/Out and Lower Power Modes
- PWR In from USB or Li-Ion Battery
- PWR Out: 1.8V, 3.3V and SYS

Benefits

- 60% Smaller than Discrete Implementation
- Single Layer Escape of BGA Signals
- Compatible with AM335x Development tools and software
- More Flexible Design
- Wide BGA ball pitch allows for low-cost assembly.
- Significantly Reduces Design Time
- Decreases Layout Complexity
- Increased Reliability through reduced number of components

Package Info

- 21mm X 21mm BGA
- 256 Balls, 1.27mm pitch
- Temp Range: 0 to 85°C

For More Information

- Contact Octavo Systems at osd335@octavosystems.com

1 Ball Map

The pins on the OSD335x-SM belong to 4 different categories, AM335x Signals, TPS65217C signals, Oscillators and Power Domains. The Oscillators and Power Domains are explained in the OSD335x-SM datasheet. The signal names for the AM335x and the TPS65217C have been named so they can be easily cross-referenced to the corresponding pin in the TI Datasheet.

All AM335x signals on the OSD335x-SM Ball Map match the signal names of the default functions in the AM335x datasheet.

All the TPS65217C signals have the prefix PMIC_ then the TPS65217C signal name from the TI Datasheet.

NOTE: This is true except for the signal PMIC_POWER_EN which is an AM335x signal.

The arrangement of the signals has been optimized for easy escape of the BGA. Table 1.1 through Table 1.4 show the ball map for the OSD335x-SM.

Table 1.1. OSD335X-SM Ball Map Top View (Columns A-D)

	A	B	C	D
16	MMC0_DAT0	MMC0_CMD	MMC0_DAT2	MII1_RXD1
15	MMC0_DAT1	MMC0_CLK	MMC0_DAT3	MII1_RXD2
14	SPI0_CS0	SPI0_D1	SPI0_CS1	MII1_RXD3
13	SPI0_SCLK	SPI0_D0	UART0_RTSN	MDC
12	UART0_RXD	UART0_TXD	UART0_CTSN	NC
11	UART1_RXD	UART1_TXD	I2C0_SDA	PMIC_SDA
10	UART1_RTSN	UART1_CTSN	I2C0_SCL	PMIC_SCL
9	AGND_ADC	VREFN	AIN6	DGND
8	AIN0	AIN1	AIN5	DGND
7	SYS_ADC_1P8V	VREFP	AIN4	AIN7
6	OSC1_IN	AIN2	AIN3	PMIC_MUX_OUT
5	OSC1_OUT	OSC1_GND	ECAP0_IN_PWM0_OUT	CAP_VDD_RTC
4	XDMA_EVENT_INTR0	XDMA_EVENT_INTR1	MCASP0_AHCLKX	EXTINTN
3	MCASP0_ACLKR	MCASP0_FSR	MCASP0_AXR1	TRSTN
2	MCASP0_FSX	MCASP0_AXR0	TDO	TMS
1	MCASP0_ACLKX	MCASP0_AHCLKR	TDI	TCK

Table 1.2. OSD335X-SM Ball Map Top View (Columns E-H)

	E	F	G	H
16	MII1_RX_CLK	MII1_RX_DV	MII1_TXD2	MII1_TX_CLK
15	MII1_RX_ER	MII1_COL	MII1_TXD3	MII1_TXD0
14	MII1_RXD0	MII1_CRS	MII1_TX_EN	MII1_TXD1
13	MDIO	VDD_MPU	VDDS_PLL	DGND
12	DGND	DGND	DGND	DGND
11	DGND	SYS_VDD2_3P3V	SYS_VDD2_3P3V	SYS_VDD_1P8V
10	DGND	SYS_VDD_1P8V	SYS_VDD_1P8V	SYS_VDD_1P8V
9	DGND	VDDSHV4	VDDSHV5	VDDSHV6
8	DGND	SYS_VDD3_3P3V	SYS_VDD3_3P3V	SYS_VDD3_3P3V
7	DGND	SYS_VDD1_3P3V	SYS_VDD1_3P3V	SYS_VDD3_3P3V
6	DGND	SYS_VDD1_3P3V	SYS_VDD1_3P3V	VPP
5	DGND	DGND	DGND	DGND
4	PMIC_NINT	VDDS_DDR	VDD_CORE	DGND
3	EMU1	LCD_VSYNC	LCD_DATA0	LCD_DATA3
2	EMU0	LCD_HSYNC	LCD_DATA1	LCD_DATA4
1	LCD_AC_BIAS_EN	LCD_PCLK	LCD_DATA2	LCD_DATA5

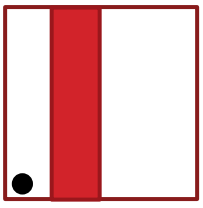


Table 1.3. OSD335X-SM Ball Map Top View (Columns J-M)

	J	K	L	M
16	USB0_VBUS	USB0_DM	USB1_DM	RTC_KALDO_ENN
15	USB0_DRVVBUS	USB0_DP	USB1_DP	USB1_VBUS
14	RMII1_REF_CLK	USB0_ID	USB1_ID	USB1_DRVVBUS
13	DGND	USB0_CE	USB1_CE	PMIC_NRESET
12	DGND	DGND	DGND	DGND
11	SYS_VDD_1P8V	SYS_RTC_1P8V	SYS_RTC_1P8V	DGND
10	SYS_VDD_1P8V	SYS_VDD_1P8V	SYS_VDD_1P8V	DGND
9	VDDSHV1	VDDSHV2	VDDSHV3	DGND
8	SYS_VDD3_3P3V	SYS_VDD3_3P3V	SYS_VDD3_3P3V	DGND
7	SYS_VDD3_3P3V	SYS_VOUT	SYS_VOUT	DGND
6	NC	SYS_VOUT	SYS_VOUT	DGND
5	DGND	DGND	DGND	DGND
4	DGND	NC	PMIC_NWAKEUP	EXT_WAKEUP
3	LCD_DATA6	LCD_DATA9	LCD_DATA12	LCD_DATA15
2	LCD_DATA7	LCD_DATA10	LCD_DATA13	EEPROM_WP
1	LCD_DATA8	LCD_DATA11	LCD_DATA14	GPMC_ADVN_ALE

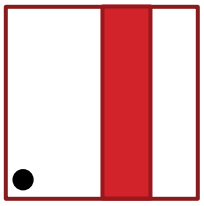
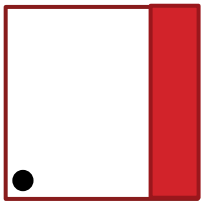


Table 1.4. OSD335X-SM Ball Map Top View (Columns N-T)

	N	P	R	T
16	OSC0_OUT	OSC0_IN	GPMC_WPN	GPMC_A11
15	OSC0_GND	GPMC_WAIT0	GPMC_A10	GPMC_A9
14	GPMC_BEN1	GPMC_A8	GPMC_A7	GPMC_A6
13	PMIC_MUX_IN	GPMC_A5	GPMC_A4	GPMC_A3
12	PMIC_PGOOD	GPMC_A2	GPMC_A1	GPMC_A0
11	PMIC_PWR_EN	PWRONRSTN	WARMRSTN	PMIC_PB_IN
10	PMIC_POWER_EN	VIN_AC	VIN_AC	VIN_AC
9	DGND	VIN_USB	VIN_USB	VIN_USB
8	DGND	VIN_BAT	VIN_BAT	VIN_BAT
7	PMIC_BAT_SENSE	GPMC_AD15	GPMC_CSN3	GPMC_CLK
6	PMIC_TS	GPMC_AD12	GPMC_AD13	GPMC_AD14
5	RTC_PWRONRSTN	GPMC_AD9	GPMC_AD10	GPMC_AD11
4	PMIC_LDO_PGOOD	GPMC_AD6	GPMC_AD7	GPMC_AD8
3	GPMC_BEN0_CLE	GPMC_CSN0	GPMC_AD0	GPMC_AD3
2	GPMC_WEN	GPMC_CSN1	GPMC_AD1	GPMC_AD4
1	GPMC_OEN_REN	GPMC_CSN2	GPMC_AD2	GPMC_AD5

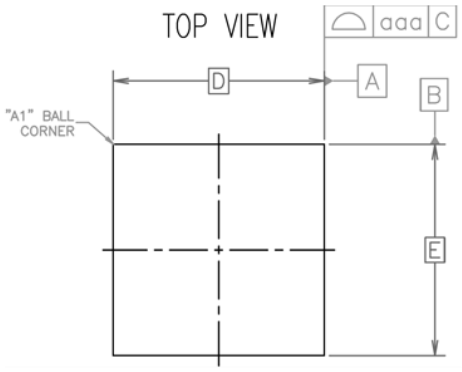


2 Packaging Information

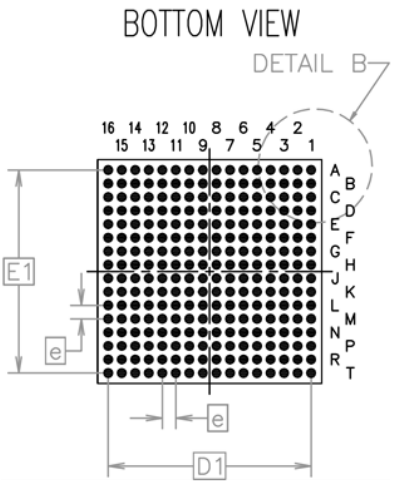
The OSD335x-SM is packaged in a 256 ball, Ball Grid Array (BGA). The package size is 21 X 21 millimeters with a ball pitch of 1.27mm. This section will give you the specifics on the package.

2.1 Mechanical Dimensions

The mechanical drawings of the OSD335x-SM show pin A1 in the upper left hand corner when looking at the top view of the device. Pin A1 is in the upper right hand corner if looking at the balls from the bottom view of the package.



DIMENSIONAL REFERENCES			
REF,	MIN.	NOM.	MAX.
A	2.82	2.95	3.08
A1	0.50	0.60	0.70
A3	1.95	2.00	2.05
D		21.00 BSC.	
D1		19.05 BSC.	
E		21.00 BSC.	
E1		19.05 BSC.	
b	0.70	0.80	0.90
c		0.35 REF.	
aaa		0.20	
bbb		0.25	
ddd		0.20	
e		1.27 BSC.	
M		16	
N		256	
Ref. JEDEC MS-034D, VARIATIONS BAH-1			



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. 'M' REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE. AND SYMBOL 'N' IS THE NUMBER OF BALLS AFTER DEPOPULATING.
4. 'b' IS MEASURABLE AT THE MAXIMUM SOLDER BALL DIAMETER AFTER REFLOW PARALLEL IMARY DATUM C .
5. DIMENSION 'ddd' IS MEASURED PARALLEL TO PRIMARY DATUM C .
6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE MATTE FINISH CHARMILLES 24 TO 27.
8. SUBSTRATE MATERIAL BASE IS BT RESIN.
9. THE OVERALL PACKAGE THICKNESS "A" ALREADY CONSIDERS COLLAPSE BALLS
10. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.