

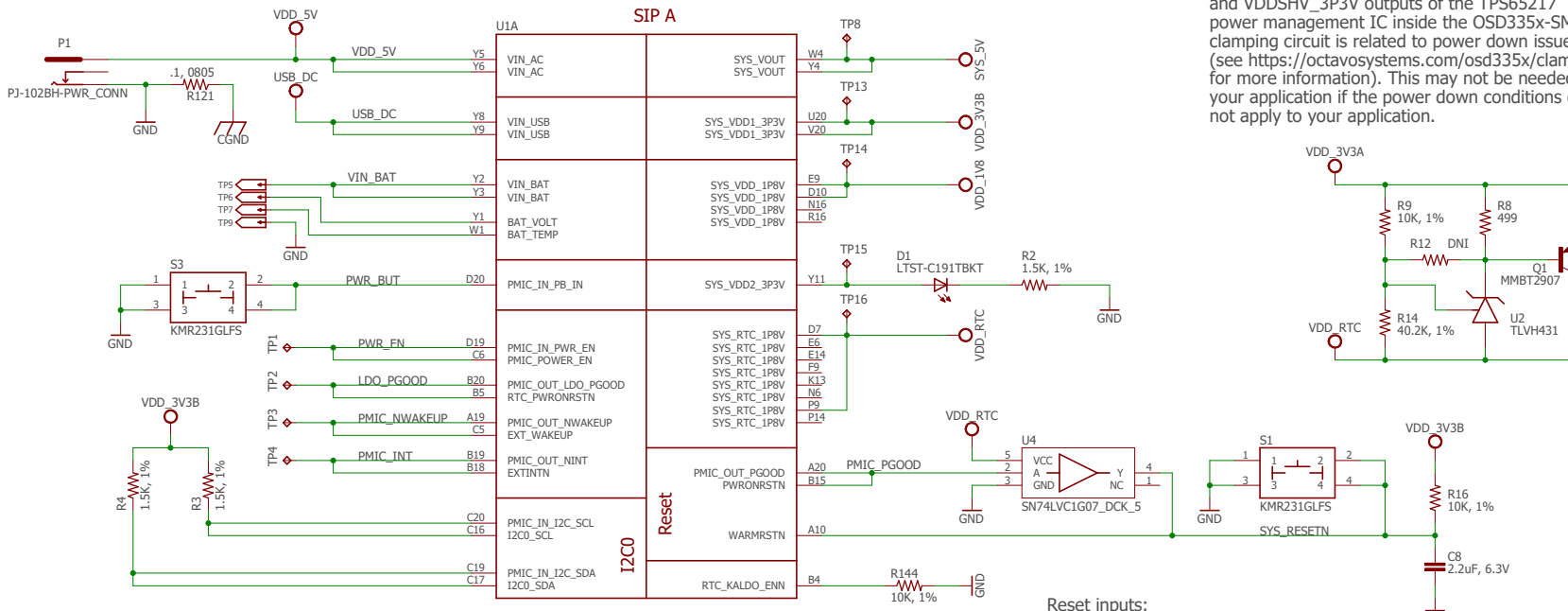
Power & Reset

Octavo Systems OSD3358-BAS SBC Reference Design

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No power input protection. Adjust according to your application.




This is a clamping circuit between the SYS_RTC_1P8V and VDDSHV_3P3V outputs of the TPS65217 power management IC inside the OSD335x-SM. The clamping circuit is related to power down issues (see <https://octavosystems.com/osd335x/clamping/> for more information). This may not be needed in your application if the power down conditions do not apply to your application.

RTC_KALDO_ENN is grounded thru a 10K ohm resistor so that the internal RTC LDO is enabled and CAP_VDD_RTC does not need to be connected to VDD_CORE.

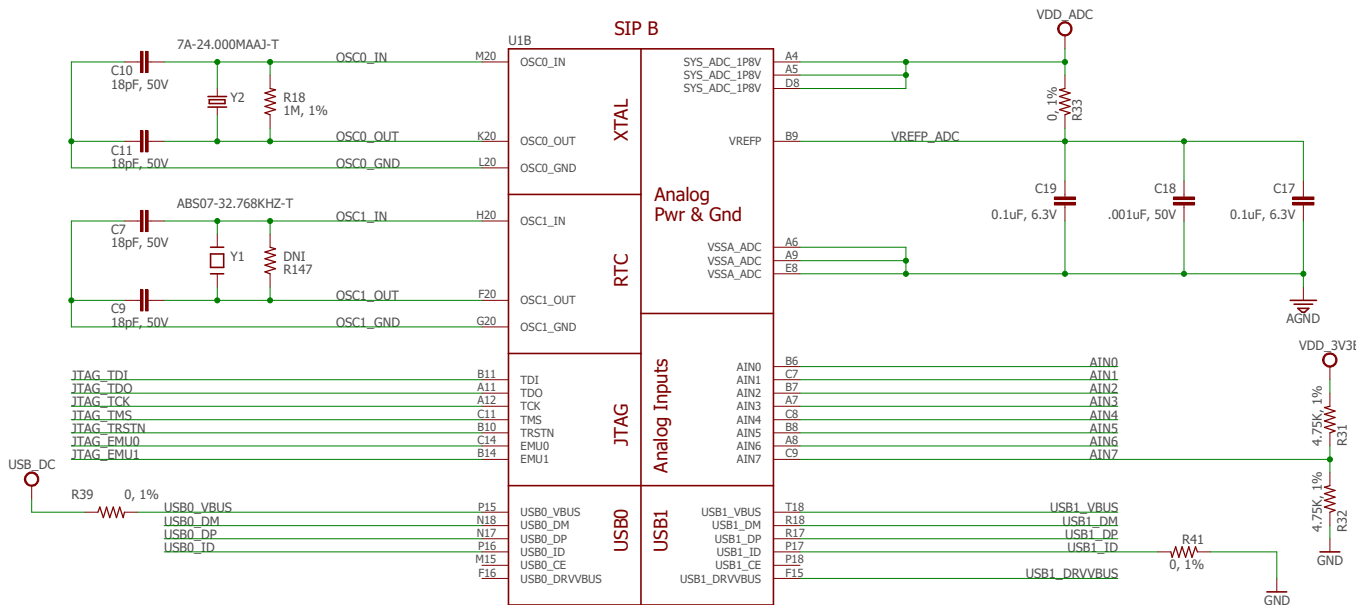
Reset inputs:
1) Manual push-button
2) PMIC_PG0OD
Each reset input is effectively open drain and can only pull reset line low.

To Print: Use 8.5"x11" paper in landscape; 0.69 scaling factor.

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Clocks & Reset

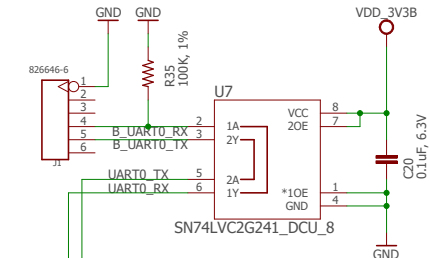
32kHz Oscillator is used for RTC. If your application does not use the RTC, then this can be removed.



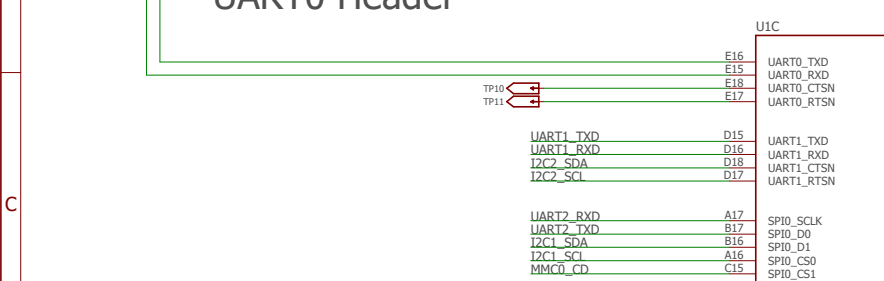
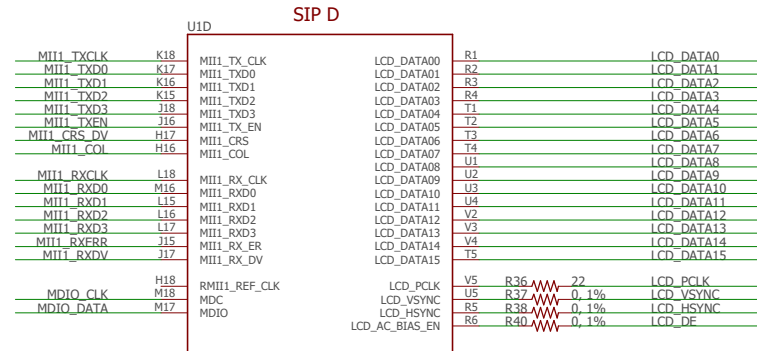
AIN7 currently monitors the 3.3V TL5209 LDO output of the OSD3358-BAS. This is not necessary and can be removed if desired. If the analog interface is not used, then VREFP should be shorted to VSSA_ADC.



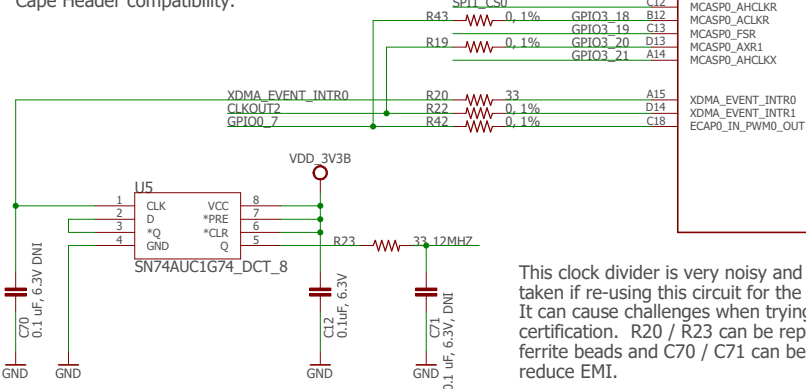
SiP Interfaces



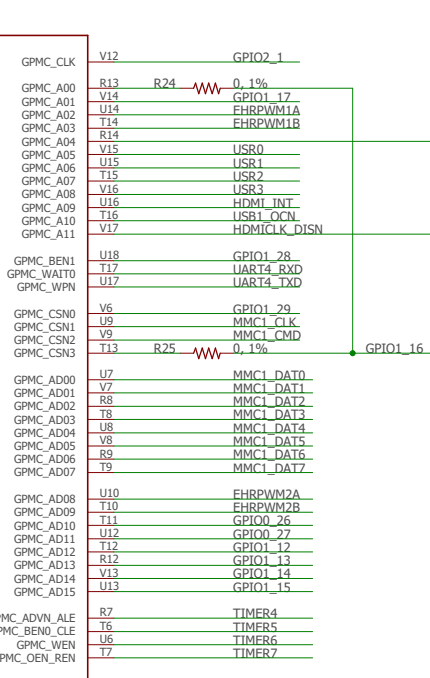
UART0 Header



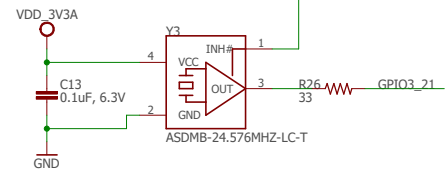
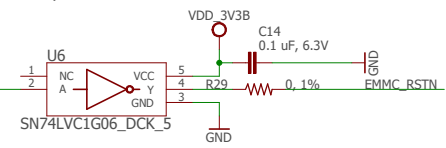
Nets like CLKOUT2, GPIO0_7 and GPIO1_16 are resistor muxed to increase the functionality of the Cape Headers. This is not needed if your application does not require Cape Header compatibility.



This clock divider is very noisy and care should be taken if re-using this circuit for the HDMI interface. It can cause challenges when trying to pass FCC / CE certification. R20 / R23 can be replaced with ferrite beads and C70 / C71 can be populated to help reduce EMI.



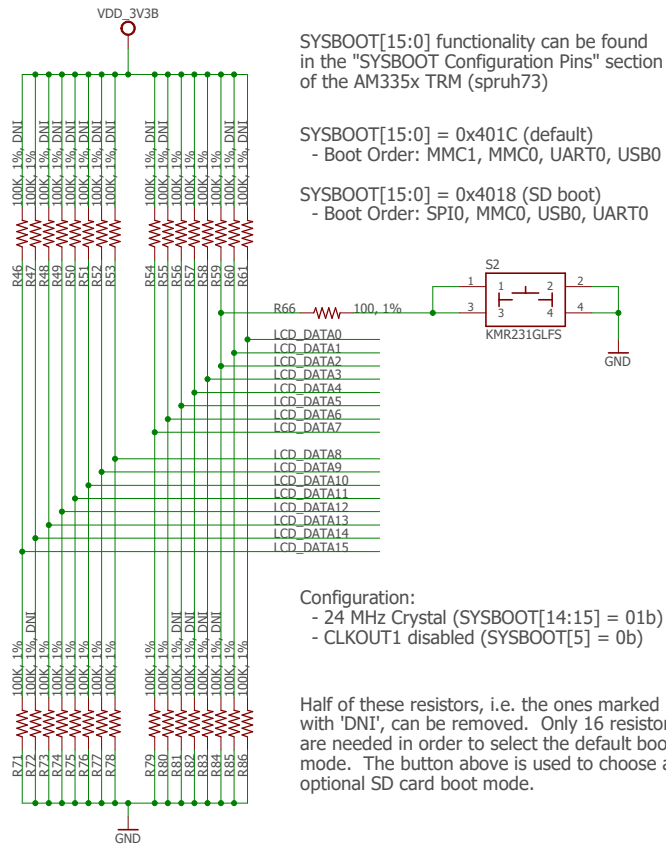
This inverter can be removed if SW is updated to change the polarity the processor drives the eMMC reset.



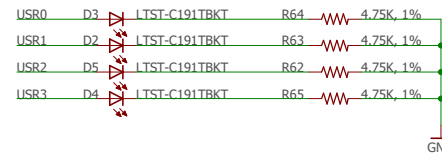
External clock to the McASP0 interface



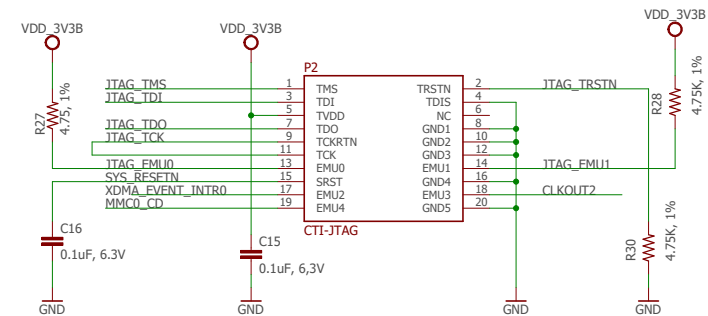
Boot configuration



User LEDs



JTAG Header

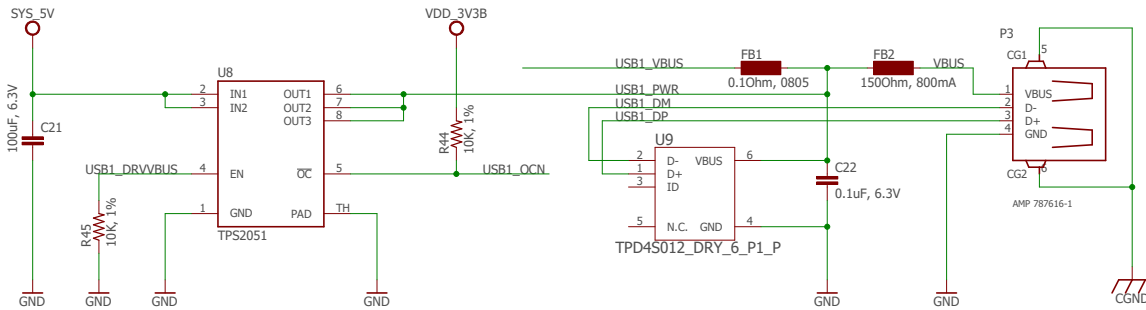


Only connect EMU2, EMU3 and EMU4 if you plan to use advanced JTAG features (HS-RTDX, Core Trace, System Trace, etc) of higher end debuggers:

- http://processors.wiki.ti.com/index.php/JTAG_Connectors
- http://processors.wiki.ti.com/index.php/XDS_Target_Connection_Guide

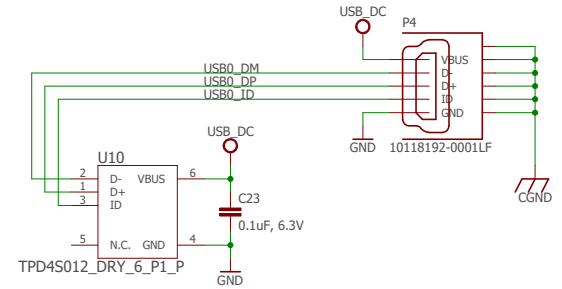


USB Host



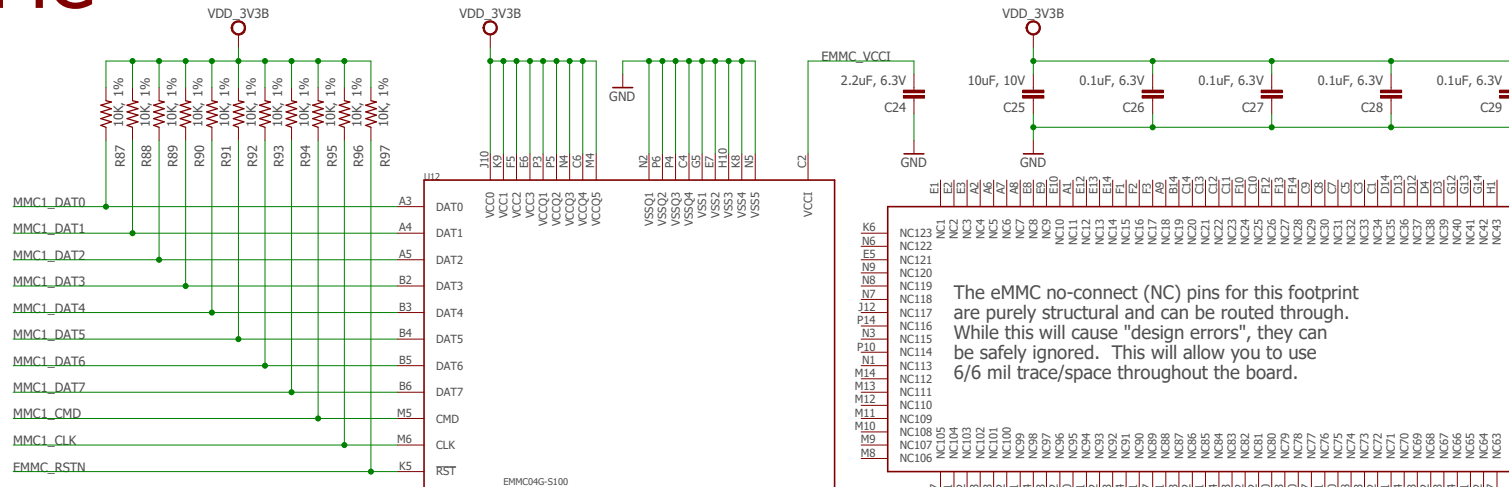
500mA current limiting switch

USB Client



In the TPD4S012, the D-, D+ and ID pins have equivalent ESD circuits and can be used interchangeably in order to make routing easier. See <http://www.ti.com/lit/gpn/tpd4s012>

eMMC

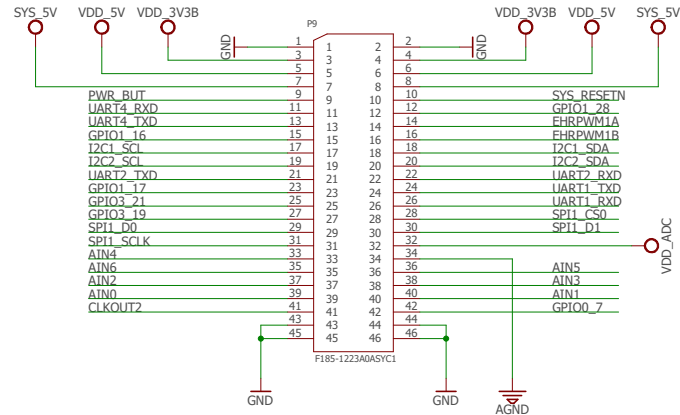
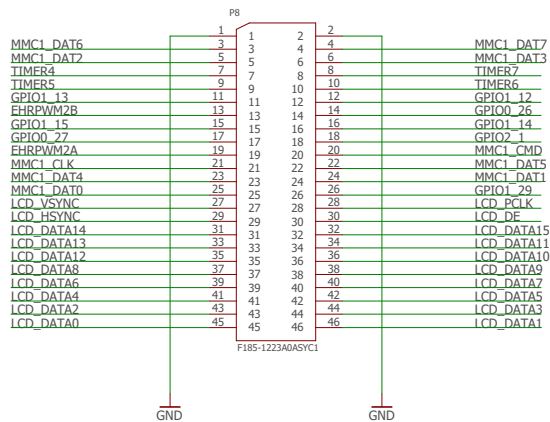


The eMMC no-connect (NC) pins for this footprint are purely structural and can be routed through. While this will cause "design errors", they can be safely ignored. This will allow you to use 6/6 mil trace/space throughout the board.

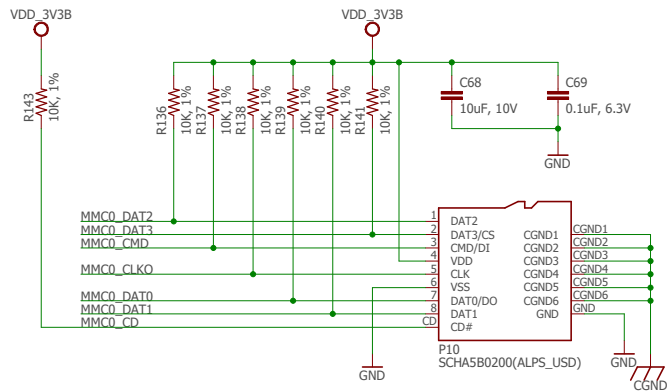
This design uses the 16GB SDIN8DE2-16G eMMC. Please choose an appropriate footprint compatible eMMC based on size and availability.



Cape Headers

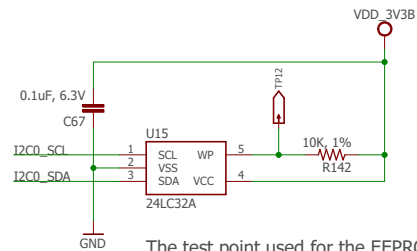


Micro SD card slot



The SCHA5B0200 is obsolete. For future designs, replace with DM3BT-DSF-PEJS or equivalent part.

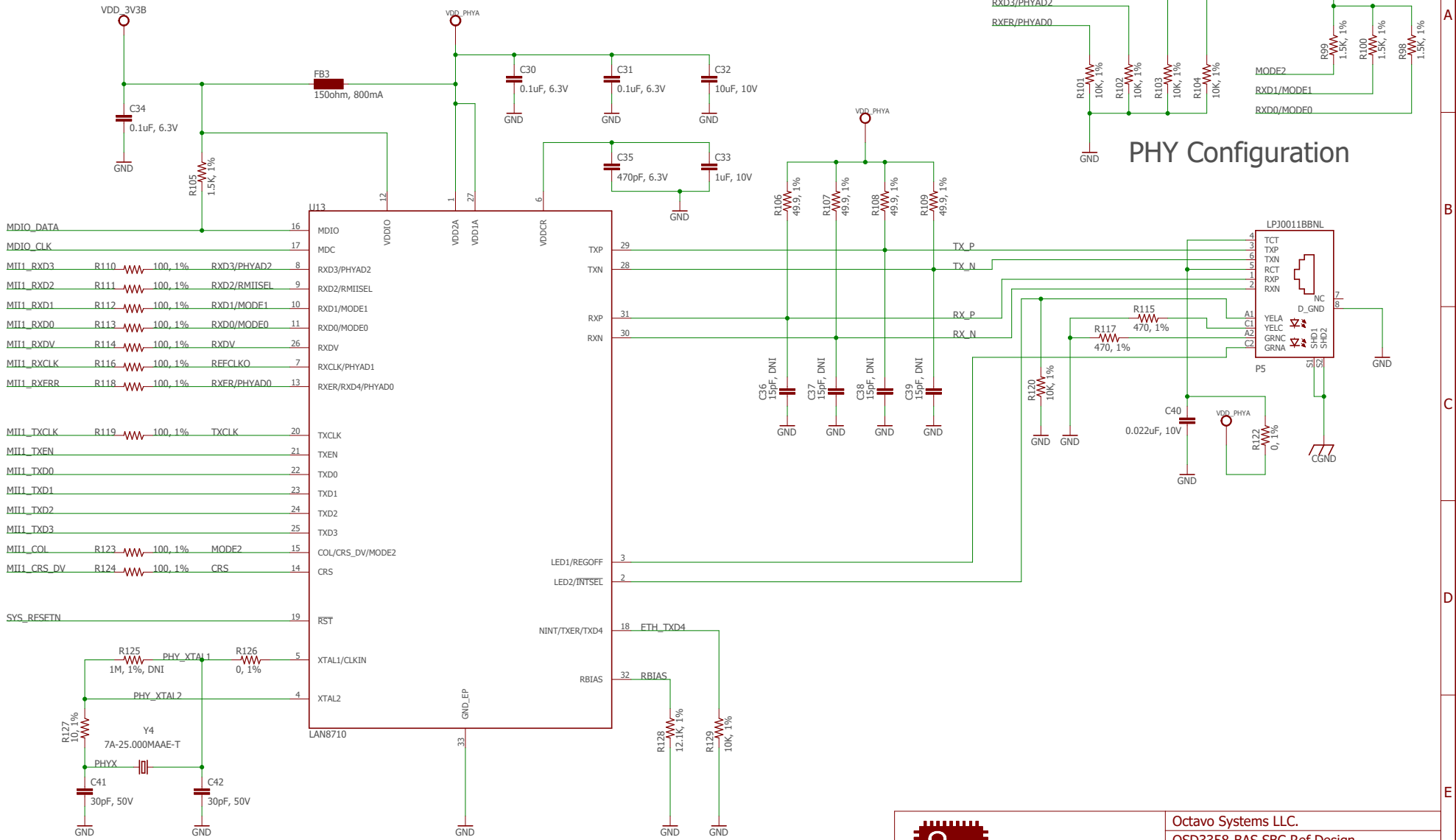
EEPROM



The test point used for the EEPROM-WP should be easily accessible and close to a ground pin. It is recommended to use a thru-hole test point so that it is easy to ground in order to program the EEPROM.

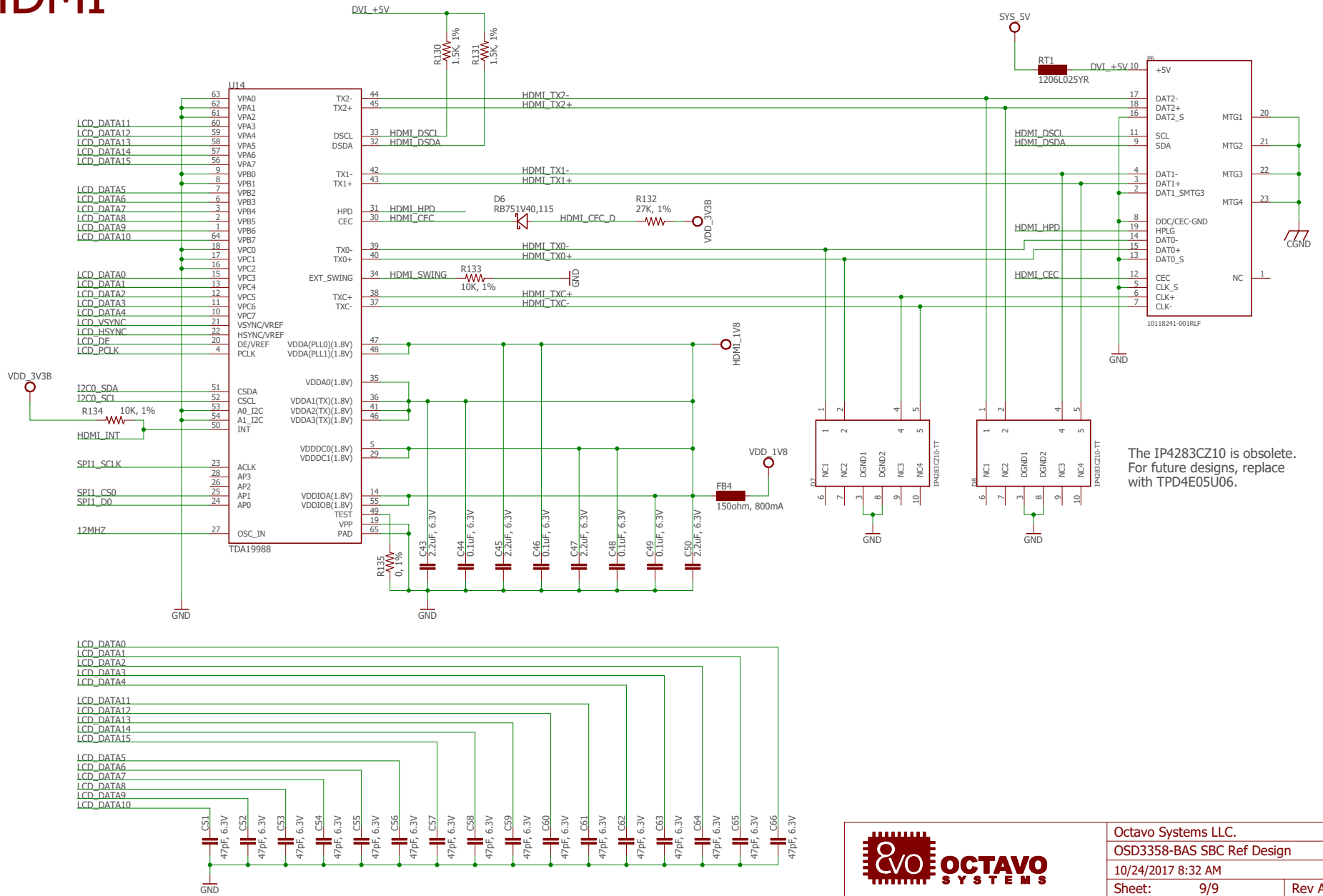


Ethernet



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HDMI



The IP4283CZ10 is obsolete.
For future designs, replace
with TPD4E05U06.

